Nokia Customer Care
3125 (RH-61) Series Transceivers

BB Description and Troubleshooting

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Baseband Overview

The baseband module of the 3125 transceiver is a CDMA single-band engine.

The cellular baseband consists of three ASICs: Universal Energy Management (UEM), Universal Phone Processor (UPP), and a 128/16 megabit combo FLASH.

The baseband architecture supports a power-saving function called *sleep mode*. This sleep mode shuts off the VCTCXO, which is used as system clock source for both RF and baseband. During the sleep mode, the system runs from a 32 kHz crystal and all the RF regulators (VR1A, VR1B, VR2, ... VR7) are off. The sleep time is determined by network parameters. Sleep mode is entered when both the MCU and the DSP are in standby mode and the normal VCTCXO clock is switched off. The phone is waken up by a timer running from this 32 kHz clock supply. The period of the sleep/wake up cycle (slotted cycle) is 1.28N seconds, where N= 0, 1, 2, depending on the slot cycle index.

The 3125 supports standard Nokia 2-wire and 3-wire chargers (ACP-x and LCH-x). However, the 3-wire chargers are treated as 2-wire chargers. The PWM control signal for controlling the 3-wire charger is ignored. The UEM ASIC and the EM SW control charging.

A BL-5C Li-ion battery is used as main power source, which has nominal capacity of 850 mAh.

Baseband and RF Architecture

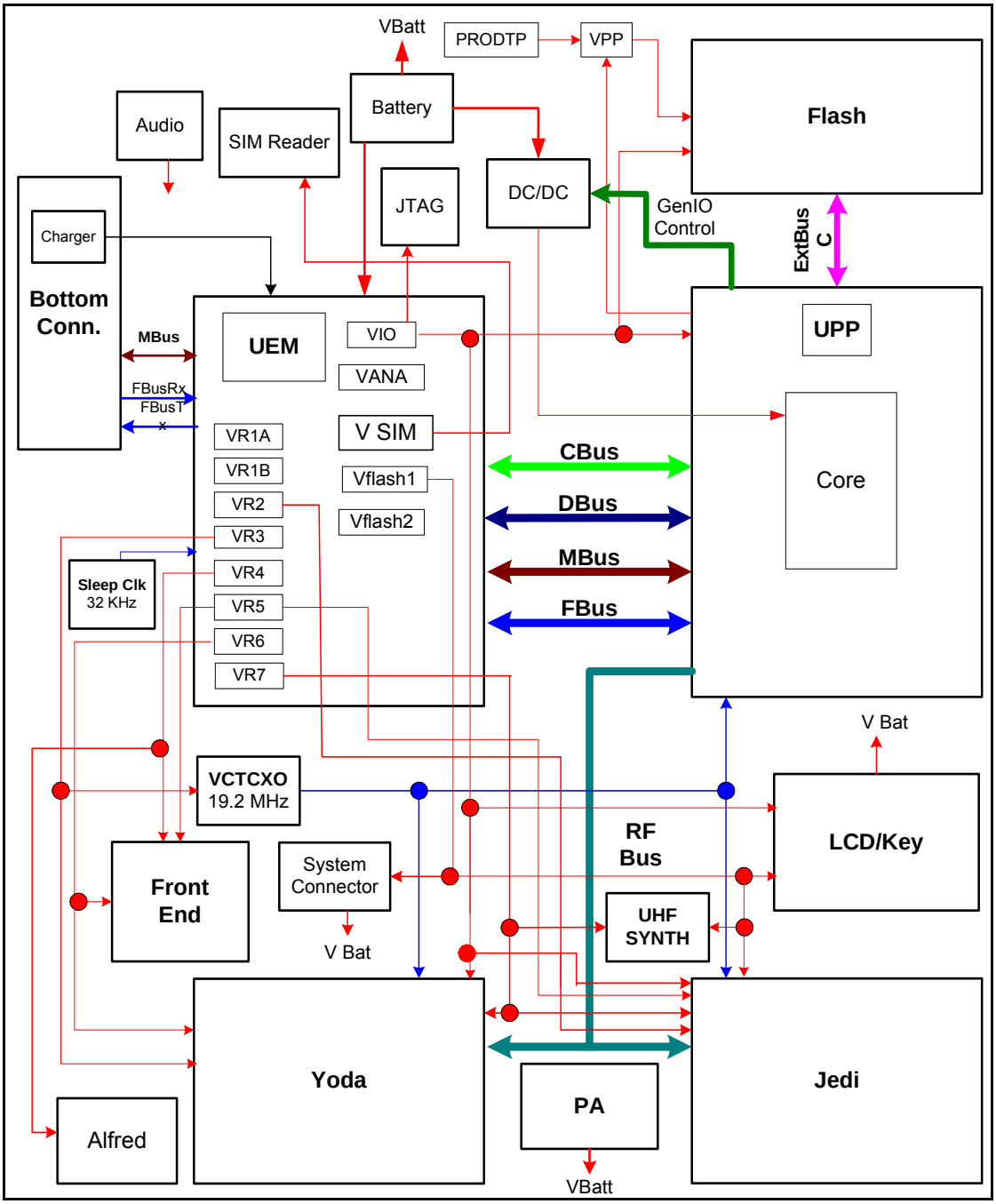


Figure 1: 3125 power distribution diagram

Power Up and Reset

Power up and reset are controlled by the UEM ASIC. The baseband can be powered up in the following ways:

- Pressing the Power button, which means grounding the PWRONX pin of the UEM
- Connecting the charger to the charger input
- Initiating the RTC Alarm, when the RTC logic has been programmed to give an alarm

After receiving one of the above signals, the UEM counts a 20 ms delay and then enters reset mode. The watchdog starts, and if the battery voltage is greater than Vcoff+, a 200 ms delay is started to allow references (etc.) to settle. After this delay elapses, the VFLASH1 regulator is enabled. Then, 500 us later, the VR3, VANA, VIO, and VCORE are enabled. Finally, the Power Up Reset (PURX) line is held low for 20 ms. This reset (PURX) is sent to the UPP. Resets are generated for the MCU and the DSP.

During this reset phase, the UEM forces the VCTCXO regulator on regardless of the status of the sleep control input signal to the UEM. The FLSRSTx from the UPP is used to reset the flash during power up and to put the flash in power down during sleep. All baseband regulators are switched on at the UEM power on, except for the SIM regulator and the Vflash2. The Vsim and Vflash2 are not used. The UEM internal watchdogs are running during the UEM reset state with the longest watchdog time selected. If the watchdog expires, the UEM returns to the power-off state. The UEM watchdogs are internally acknowledged at the rising edge of the PURX signal to always give the same watchdog response time to the MCU.

The following timing diagram represents the UEM start-up sequence from reset to power-on mode.

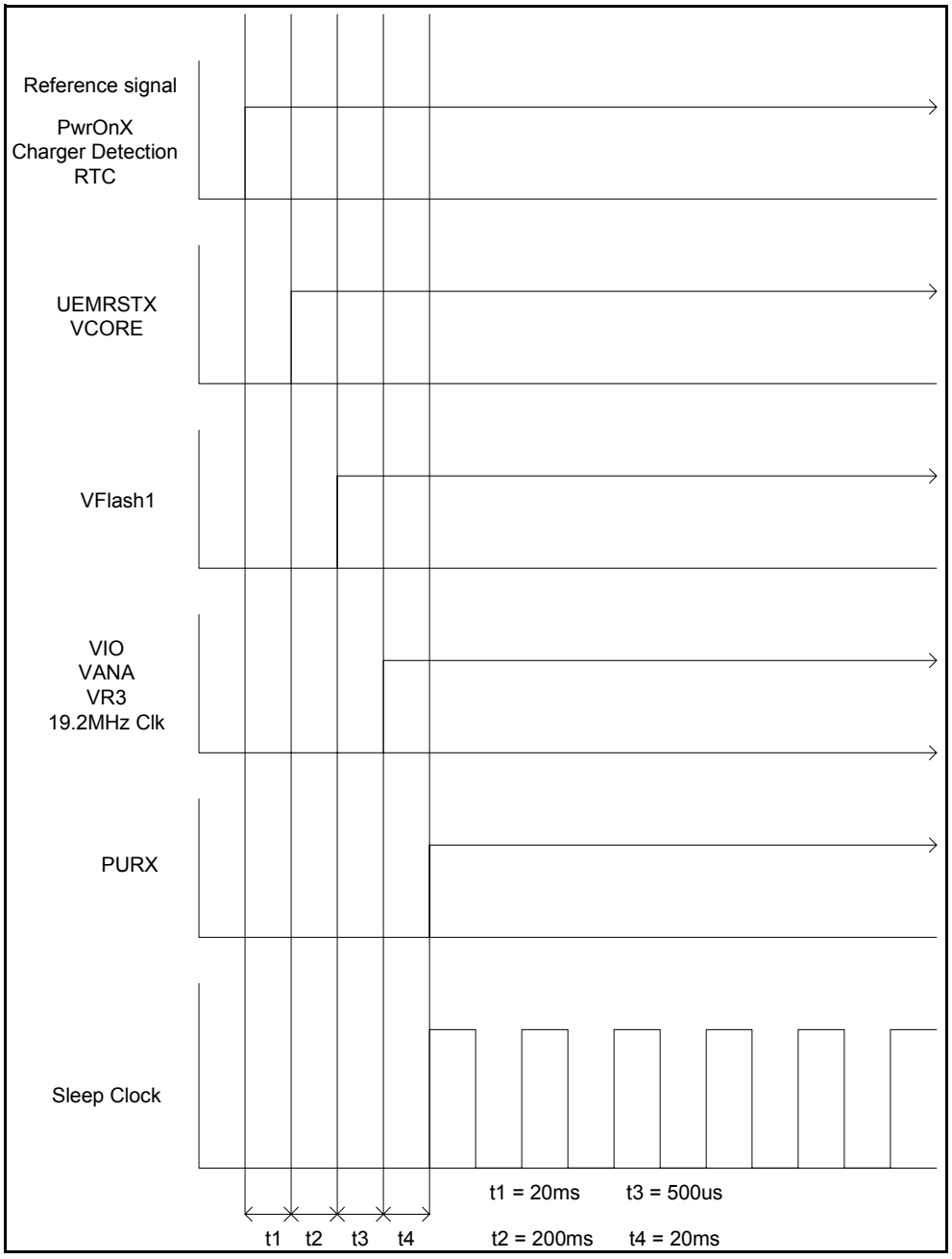


Figure 2: Power-on sequence and timing

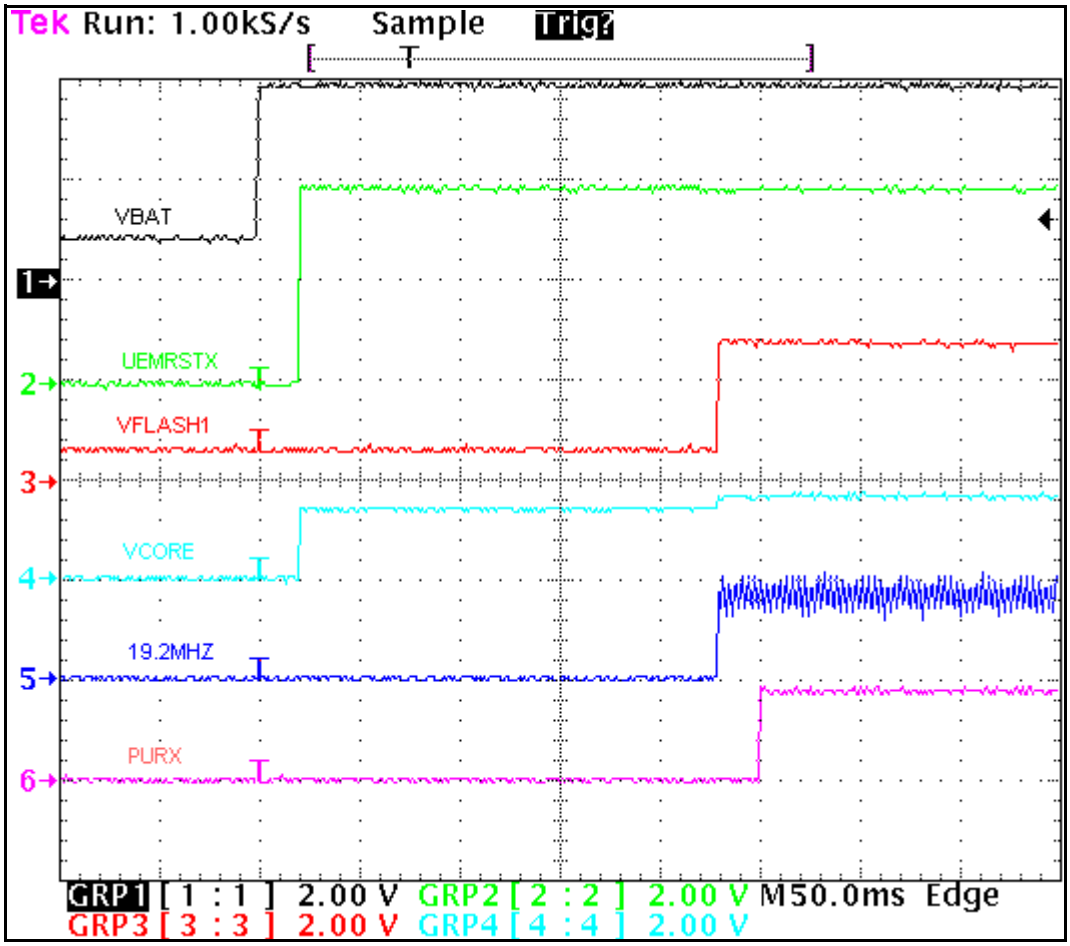


Figure 3: Measured power-on sequence and timing

Power Up – Power Key

When the Power key is pressed, the UEM enters the power-up sequence. Pressing the Power key causes the PWRONX pin on the UEM to be grounded. The UEM PWRONX signal is not part of the keypad matrix. The Power key is only connected to the UEM. This means that when pressing the power key an interrupt is generated to the UPP that starts the MCU. The MCU then reads the UEM interrupt register and notices that it is a PWRONX interrupt. The MCU reads the status of the PWRONX signal using the UEM control bus (CBUS). If the PWRONX signal stays low for a certain time the MCU accepts this as a valid power-on state and continues with the SW initialization of the baseband. If the Power key does not indicate a valid power-on situation, the MCU powers off the baseband.

Power Up – Charger

In order to be able to detect and start charging in cases where the main battery is fully discharged (empty) and the UEM has no supply (NO_SUPPLY or BACKUP mode of UEM), charging is controlled by *start-up charging* circuitry.

Whenever the VBAT level is detected to be below the master reset threshold (V_{MSTR-}), charging is controlled by start-up charging circuitry. Connecting a charger forces the

VCHAR input to rise above the charger detection threshold (VCH_{DET+}) and by detection, start-up charging is initiated. The UEM generates 100 mA constant output current from the connected charger's output voltage. The battery's voltage rises at it charges, and when the VBAT voltage level is detected to be higher than the master reset threshold limit (V_{MSTR+}), the start-up charge is terminated.

Monitoring the VBAT voltage level is done by a charge control block (CHACON). A MSTRX='1' output reset signal (internal to the UEM) is given to the UEM's RESET block when the VBAT>V_{MSTR+} and the UEM enters into the reset sequence.

If the VBAT is detected to fall below V_{MSTR} during start-up charging, charging is cancelled. It will restart if a new rising edge on the VCHAR input is detected (VCHAR rising above VCH_{DET+}).

Power Up - RTC Alarm

If the phone is in power-off mode when an RTC alarm occurs, the wake-up procedure occurs. After the baseband is powered on, an interrupt is given to the MCU. When an RTC alarm occurs during active mode, the interrupt is generated to the MCU.

Power Off

The baseband switches to power-off mode if any of following occurs:

- Power key is pressed
- Battery voltage is too low (VBATT < 3.2 V)
- Watchdog timer register expires

The UEM controls the power-down procedure.

Power Consumption and Operation Modes

In POWER-OFF mode, the power (VBAT) is supplied to the UEM, buzzer, vibra, LED, PA, and PA drivers. During this mode, the current consumption is approximately 35 uA.

In Sleep Mode, both processors (MCU and DSP) are in stand-by mode. The phone enters sleep mode only when both processors make this request. When the SLEEPX signal is detected low by the UEM, the phone enters SLEEP mode. The VIO and VFLASH1 regulators are put into low quiescent current mode, VCORE enters LDO mode, and the VANA and VFLASH2 regulators are disabled. All RF regulators are disabled during SLEEP mode. When the SLEEPX signal is detected high by the UEM, the phone enters ACTIVE mode and all functions are activated.

Sleep mode is exited either by the expiration of a sleep clock counter in the UEM or by some external interrupt (generated by a charger connection, key press, headset connection, etc.).

In sleep mode, the VCTCXO is shut down and the 32 kHz sleep clock oscillator is used as a reference clock for the baseband.

The average current consumption of the phone in sleep mode can vary depending mainly on the SW state (e.g., slot cycle 0, 1, or 2) and if the phone is working on IS95 or IS2000 for CDMA. However, the average consumption is about 6 mA in slot cycle 0 on IS95.

In the Active Mode, the phone is in normal operation, scanning for channels, listening to a base station, transmitting and processing information. There are several sub-states in the active mode depending on the present state of the phone, such as burst reception, burst transmission, if the DSP is working, etc.

In active mode, SW controls the VR1A and VR1B UEM RF regulators, which can be enabled or disabled. VSIM can be enabled or disabled and its output voltage can be programmed to be 1.8 V or 3.3 V. VR2 and VR4—VR7 can be enabled, disabled, or forced into low quiescent current mode. VR3 is always enabled in active mode and disabled during sleep mode and cannot be controlled by SW in the same way as the other regulators. VR3 will only turn off if both processors request to be in sleep mode.

Charging Mode can be performed in parallel with any other operating mode. A BSI resistor inside the battery pack indicates the battery type/size. The resistor value corresponds to a specific battery capacity. This capacity value is related to the battery technology.

The battery voltage, temperature, size, and charging current are measured by the UEM and the charging software running in the UPP controls it.

The charging control circuitry (CHACON) inside the UEM controls the charging current delivered from the charger to the battery and phone. The battery voltage rise is limited by turning the UEM switch off when the battery voltage has reached 4.2 V. The charging current is monitored by measuring the voltage drop across a 220 mOhm resistor.

Power Distribution

In normal operation, the baseband is powered from the phone's battery. The battery consists of one Lithium-Ion cell capacity of 850 mAh and some safety and protection circuits to prevent harm to the battery.

The UEM ASIC controls the power distribution to the whole phone through the BB and RF regulators excluding the power amplifier (PA), which has a continuous power rail directly from the battery. The battery feeds power directly to the following parts of the system:

- UEM
- PA
- Buzzer
- Vibra
- Display
- Keyboard lights

The heart of the power distribution to the phone is the power control block inside the

UEM. It includes all the voltage regulators and feeds the power to the whole system. The UEM handles hardware power-up functions so the regulators are not powered and the power up reset (PURX) is not released if the battery voltage is less than 3 V.

The baseband is powered from five different UEM regulators.

Table 1: Baseband Regulators

Regulator	Maximum Current (mA)	Vout (V)	Notes
VCORE	300 400	1.5 1.35	Output voltage selectable 1.0V/1.3V. Power up default value is 1.35V.
VIO	150	1.8	Enabled always except during power-off mode
VFLASH1	70	2.78	Enabled always except during power-off mode
VFLASH2	40	2.78	Enabled only when data cable is connected
VANA	80	2.78	Enabled only when the system is awake (Off during sleep and power off-modes)
VSIM	25	3.0	Enabled only when SIM card is used

Table 2 includes the UEM regulators for the RF.

Table 2: RF Regulators

Regulator	Maximum Current (mA)	Vout (V)	Notes
VR1A	10	4.75	Enabled when cell transmitter is on
VR1B	10	4.75	Enabled when the transmitter is on
VR2	100	2.78	Enabled when the transmitter is on
VR3	20	2.78	Enabled when SleepX is high
VR4	50	2.78	Enabled when the receiver is on
VR5	50	2.78	Enabled when the receiver is on
VR6	50	2.78	Enabled when the transmitter is on
VR7	45	2.78	Enabled when the receiver is on

The charge pump that is used by VR1A is constructed around the UEM. The charge pump works with the Cbus (1.2 MHz) oscillator and gives a 4.75 V regulated output voltage to the RF.

Clock Distribution

RFClk (19.2 MHz Analog)

The main clock signal for the baseband is generated from the voltage and temperature controlled crystal oscillator VCTCXO (G500). This 19.2 MHz clock signal is generated at the RF and is fed to Yoda pin 18 (TCXO_IN) at C711. Yoda then converts the analog sine waveform to a digital waveform with a swing voltage of 0 tot 1.8 V and sends it to the UPP from pin 16 at Yoda (19.2 Out) to the UPP pin M5 (RFCLK).

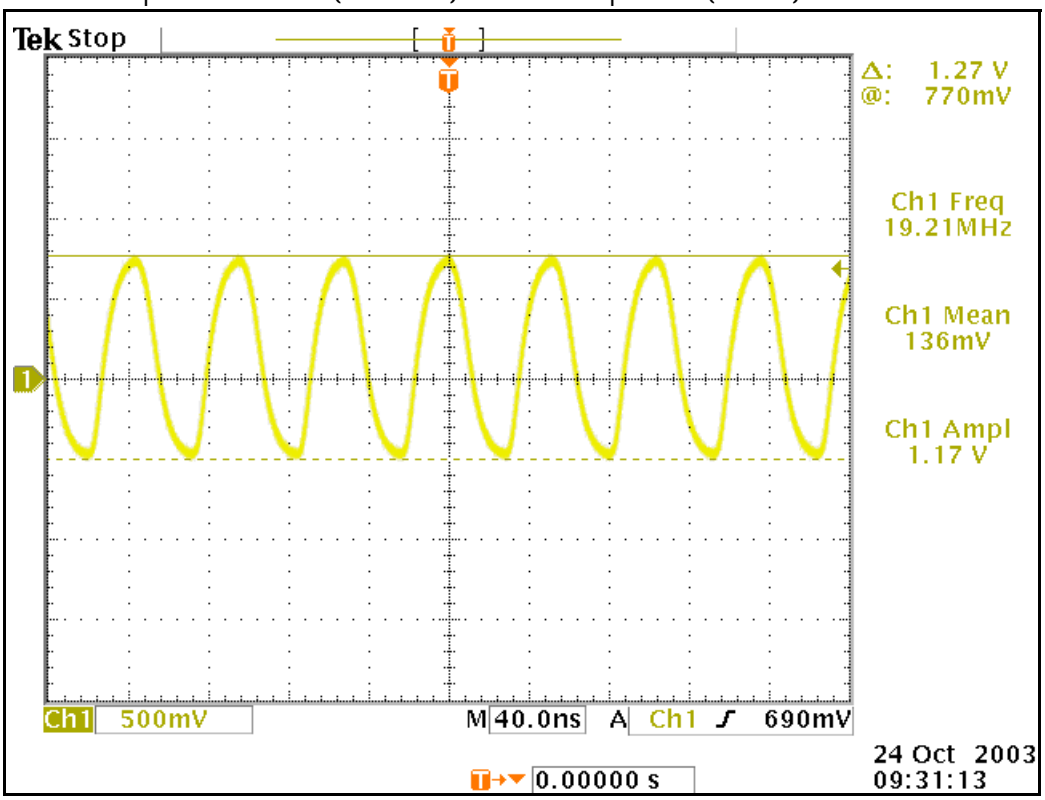


Figure 4: Waveform of the 19.2 MHz clock (VCTCXO) going to the Yoda ASIC

Figure 5 shows the RFCLK signal for the UPP.

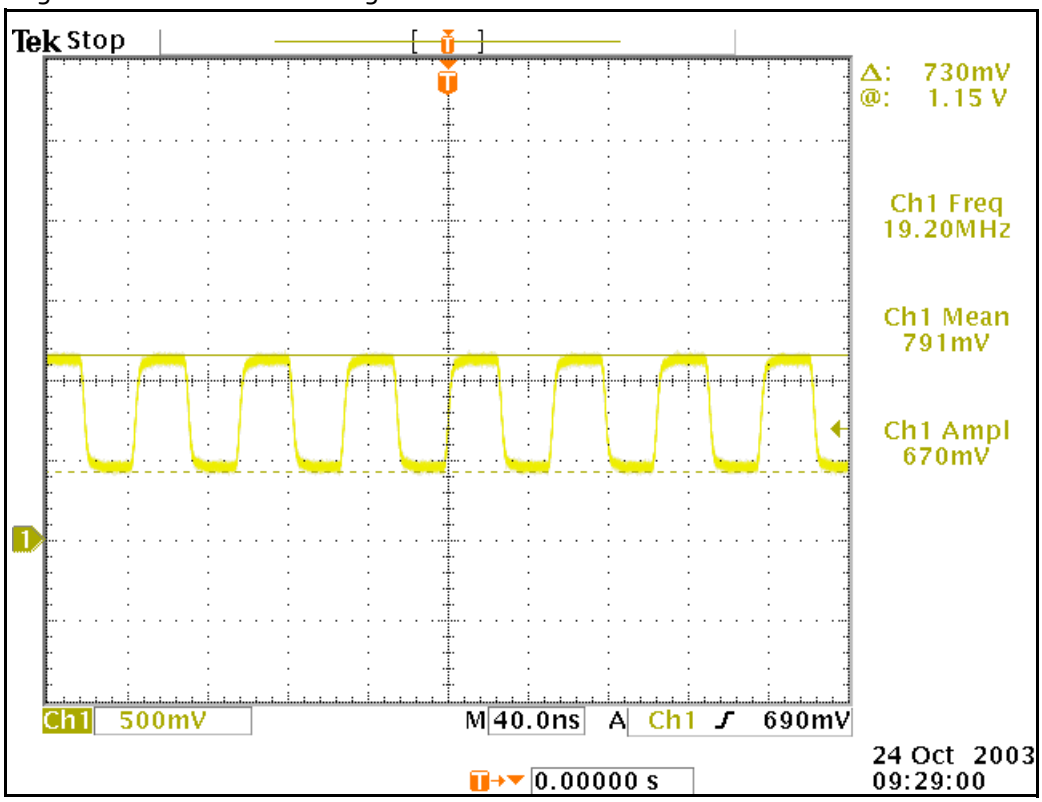


Figure 5: Waveform of the 19.2 MHz Clk going to the UPP for Yoda ASIC

RFConvClk (19.2 MHz digital)

The UPP distributes the 19.2 MHz internal clock to the DSP and MCU, where the SW multiplies this clock by seven for the DSP and by two for the MCU.

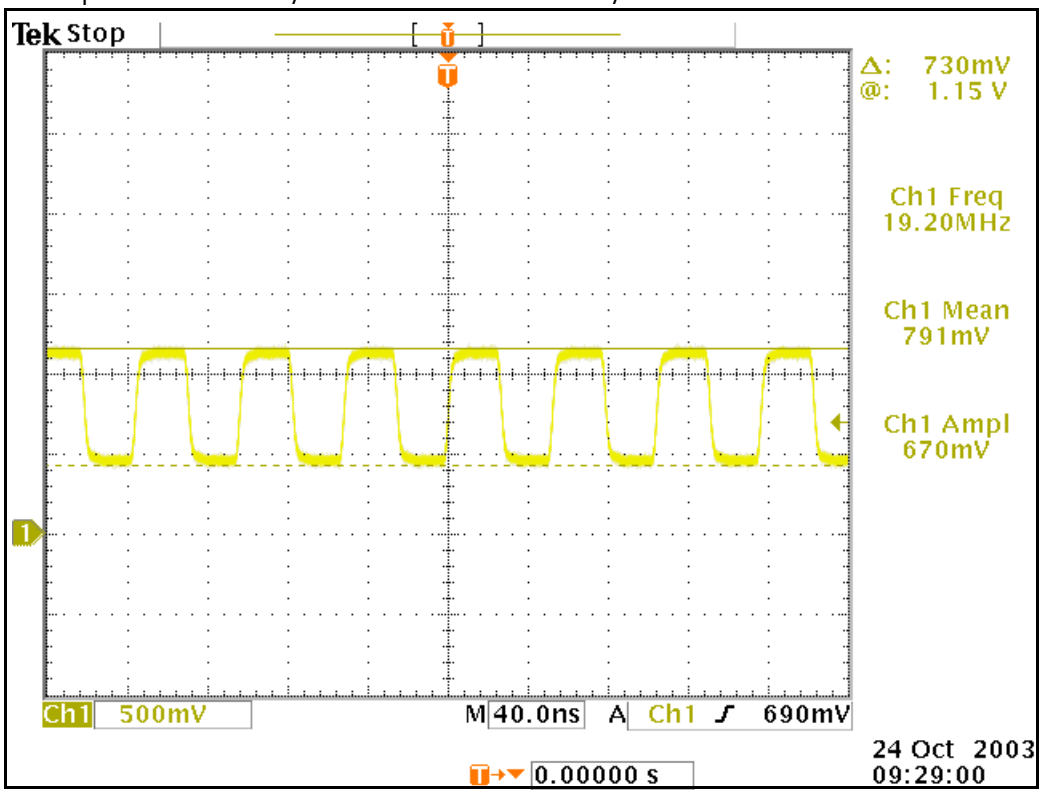


Figure 6: RFCovCLk waveform

CBUSClk Interface

A 1.2 MHz clock signal is used for CBUS, which is used by the MCU to transfer data between the UEM and UPP.

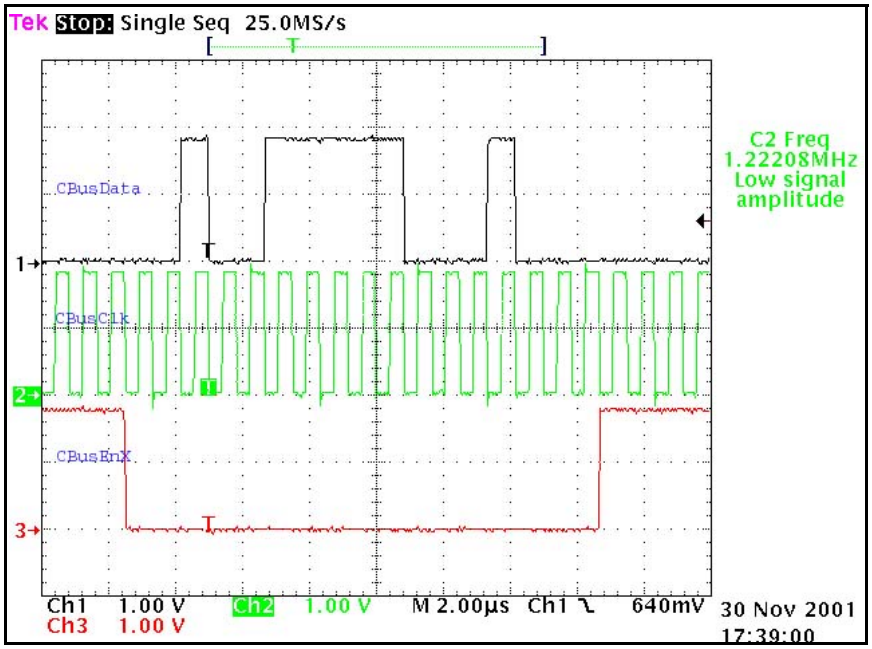


Figure 7: Cbus Data Transfer

DBUS Clk Interface

A 9.6 MHz clock signal is used for DBUS, which is used by the DSP to transfer data between the UEM and UPP.

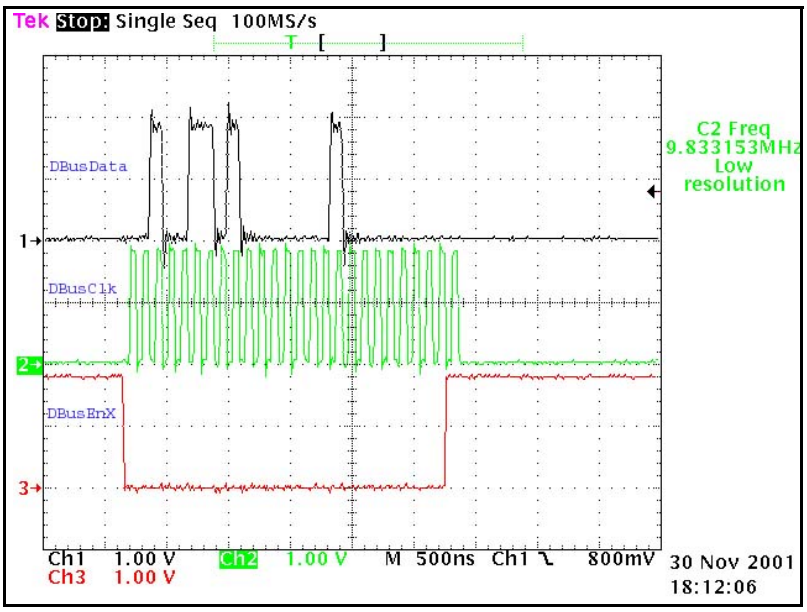


Figure 8: Dbus data transferring

The system clock is stopped during sleep mode by disabling the VCTCXO power supply (VR3) from the UEM regulator output by turning off the controlled output signal SleepX from the UPP.

SleepCLK (Digital)

The UEM provides a 32 kHz sleep clock for internal use and to the UPP, where it is used for sleep mode timing.

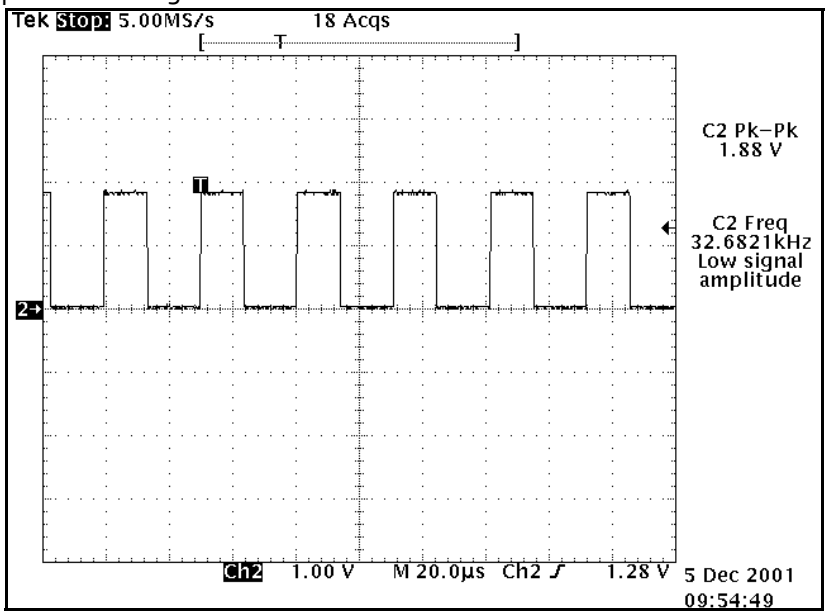


Figure 9: 32 kHz Digital output from UEM

SleepCLK (Analog)

When the system enters sleep mode or power off mode, the external 32 KHz crystal provides a reference to the UEM RTC circuit to turn on the phone during power off or sleep mode.

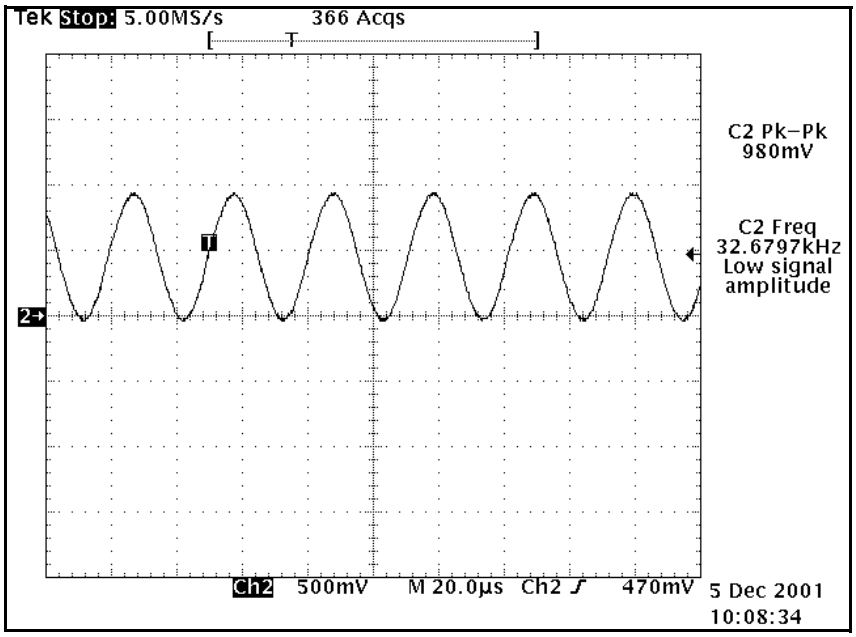


Figure 10: 32 kHz analog waveform at 32 KHz crystal input

Flash Programming

Connections to Baseband

The flash programming equipment is connected to the baseband using test pads for galvanic connection. The test pads are allocated in such a way that they can be accessed when the phone is assembled. The flash programming interface uses the VPP, FBUSTX, FBUSRX, MBUS, and BSI connections for the connection to the baseband. The connection is through the UEM, which means that the logic levels corresponding to 2.7 V. Power is supplied using the battery contacts.

Baseband Power Up

The baseband power is controlled by the flash prommer in production and in reprogramming situations. The baseband powers up by applying supply voltage to the battery terminals. Once the baseband is powered, flash programming indication begins (see the following "Flash Programming Indication" section).

Flash Programming Indication

Flash programming is indicated to the UPP using the MBUSRX signal between the UPP and UEM. The MBUS signal from the baseband to the flash prommer is used as a clock for the synchronous communication. The flash prommer keeps the MBUS line low during UPP boot to indicate that the flash prommer is connected. If the UPP MBUSRX signal is low on UPP, the MCU enters flash programming mode. In order to avoid accidental entry to the flash-programming mode, the MCU waits for a specified time to get input data from the flash prommer. If the timer expires without any data being received, the MCU

continues the boot sequence. The MBUS signal from the UEM to the external connection is used as a clock during flash programming. This means that the flash-programming clock is supplied to the UPP on the MBUSRX signal.

The flash prommer indicates flash programming/reprogramming to the UEM by writing an 8-bit password to the UEM. The data is transmitted on the FBUSRX line and the UEM clocks the data on the FBUSRX line into a shift register. When the 8 bits have been shifted in the register, the flash prommer generates a falling edge on the BSI line. This loads the shift register content in the UEM into a compare register. If the 8 bits in the compare register matches with the default value preset in the UEM, the flash prommer pulls the MBUS signal to UEM low in order to indicate to the MCU that the flash prommer is connected. The UEM reset state machine performs a reset to the system, PURX low, for 20 ms. The UEM flash programming mode is valid until the MCU sets a bit in the UEM register that indicates the end of flash programming. Setting this bit also clears the compare register in the UEM, which was loaded at the falling edge of the BSI signal. The UEM watchdogs are disabled during the flash programming mode. Setting the bit indicating the end of flash programming enables and resets the UEM watchdog timer to its default value. Clearing the flash programming bit also causes the UEM to generate a reset to the UPP.

The BSI signal is used to load the value into the compare register. In order to avoid spurious loading of the register, the BSI signal is gated during UEM master reset and during power on when PURX is active. The BSI signal should not change states during normal operation unless the battery is extracted. In this case, the BSI signal will be pulled high. Note that a falling edge is required to load the compare register.

Flashing

Flash programming is done through the VPP, FBUSTX, FBUSRX, MBUS, and BSI signals. When the phone enters the flash programming mode, the prommer indicates to the UEM that flash programming will take place by writing an 8-bit password to the UEM. The prommer sets the BSI value to “1” and then uses FBUSRX for writing and MBUS for clocking. The BSI is then set back to “0”.

The MCU uses the FBUSTX signal to indicates to the prommer that it has been noticed. After this, it reports the UPP type ID and is ready to receive the secondary boot code to its internal SRAM.

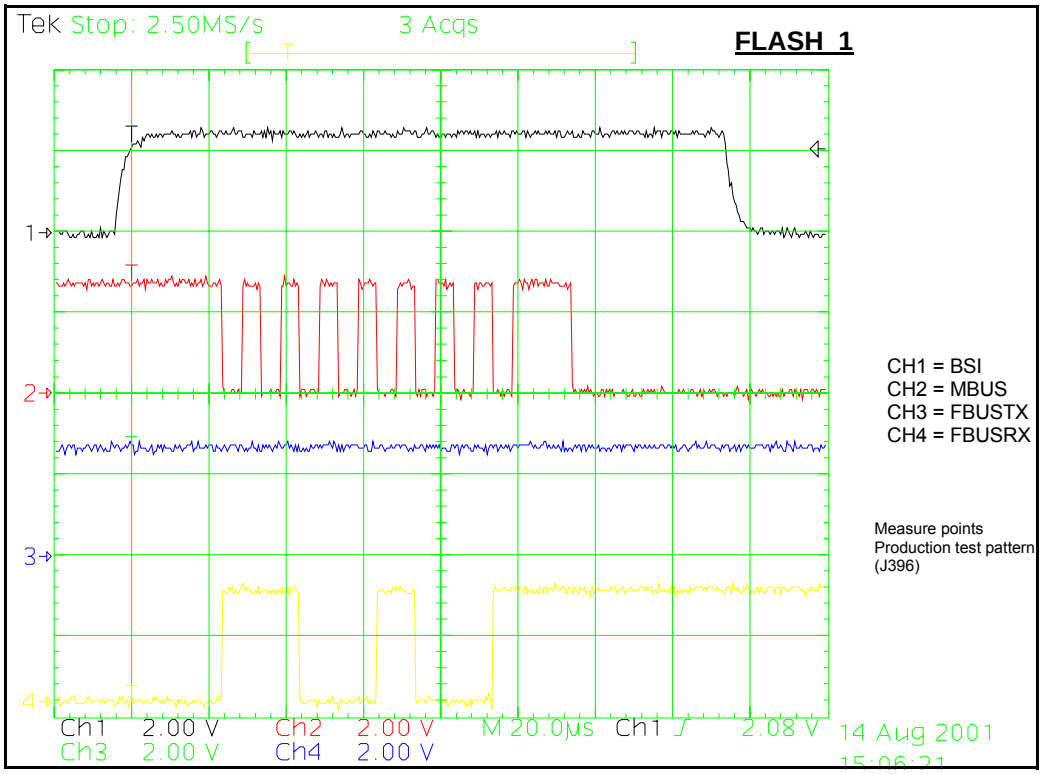


Figure 11: Flashing starts by BSI being pulled up and password being sent to UEM

This boot code asks the MCU to report the phone's configuration information to the prommer, including the flash device type. The prommer can then select and send algorithm code to the MCU SRAM (and SRAM/Flash self-tests can be executed).

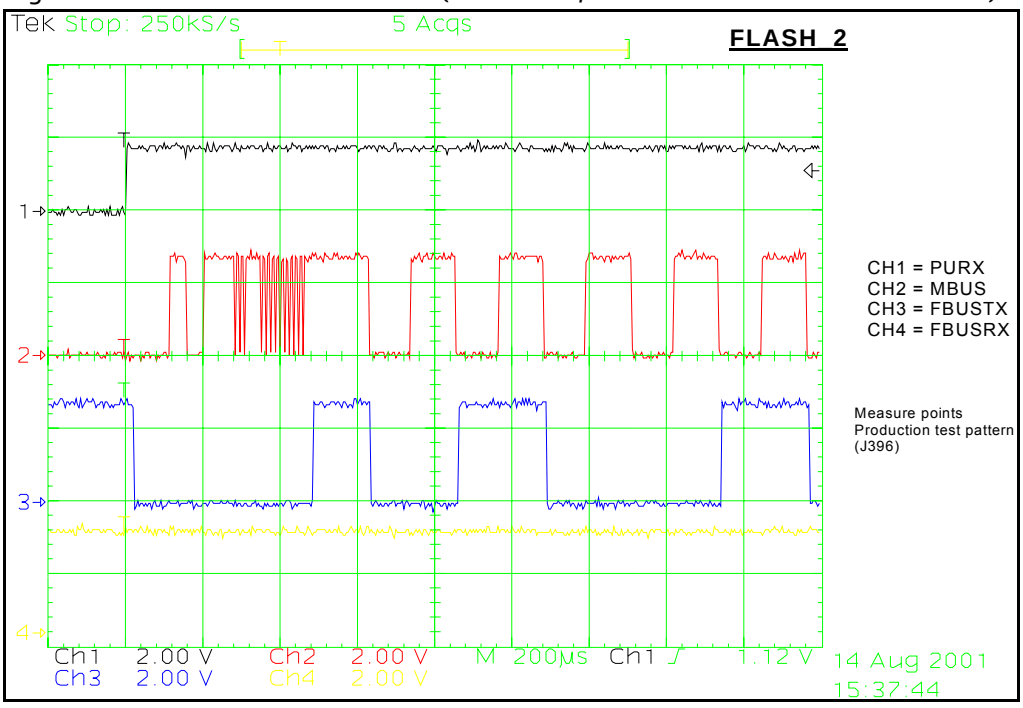


Figure 12: Flashing, continued

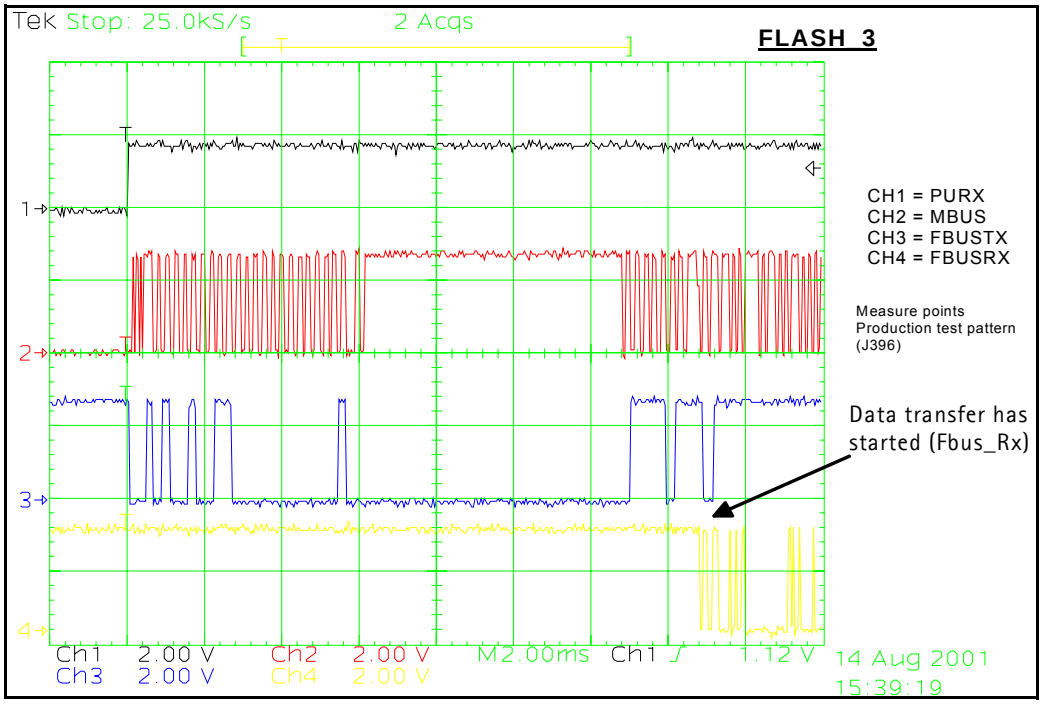


Figure 13: Flashing, continued 2

Flash Programming Error Codes

The following characteristics apply to the information in Table 3.

- Error codes can be seen from the test results or from Phoenix's flash-tool.
- Underlined information means that the connection under consideration is being used for the first time.

Table 3: Flash Programming Error Codes

Error	Description	Not Working Properly
C101	"The Phone does not set FbusTx line high after the startup."	Vflash1 VBatt BSI and FbusRX from prommer to UEM. FbusTx from UPP->UEM->Prommer(SA0)
C102	"The Phone does not set FbusTx line low after the line has been high. The Prommer generates this error also when the Phone is not connected to the Prommer."	PURX(also to Safari) VR3 Rfclock(VCTCXO->Safari->UPP) Mbus from Prommer->UEM->UPP(MbusRx)(SA0) FbusTx from UPP->UEM->Prommer(SA1) BSI and FbusRX from prommer to UEM.
C103	" Boot serial line fail."	Mbus from Prommer->UEM->UPP(MbusRx)(SA1) FbusRx from Prommer->UEM->UPP FbusTx from UPP->UEM->Prommer
C104	"MCU ID message sending failed in the Phone."	FbusTx from UPP->UEM->Prommer

Table 3: Flash Programming Error Codes (Continued)

Error	Description	Not Working Properly
C105	"The Phone has not received Secondary boot codes length bytes correctly."	Mbus from Prommer->UEM->UPP(MbusRx) FbusRx from Prommer->UEM->UPP FbusTx from UPP->UEM->Prommer
C106	"The Phone has not received Secondary code bytes correctly."	Mbus from Prommer->UEM->UPP(MbusRx) FbusRx from Prommer->UEM->UPP FbusTx from UPP->UEM->Prommer
C107	"The Phone MCU can not start Secondary code correctly."	UPP
C586	"The erasing status response from the Phone informs about fail."	Flash
C686	"The programming status response from the Phone informs about fail."	Flash
Cx81	"The Prommer has detected a checksum error in the message, which it has received from the Phone."	FbusTx from UPP->UEM->Prommer
Cx82	"The Prommer has detected a wrong ID byte in the message, which it has received from the Phone."	FbusTx from UPP->UEM->Prommer
A204 Cx83 Cx84 Cx85	"The flash manufacturer and device IDs in the existing algorithm files do not match with the IDs received from the target phone." "The Prommer has not received phone acknowledge to the message." "The phone has generated NAK signal during data block transfer." "Data block handling timeout"	Flash UPP VIO/VANA Signals between UPP-Flash Mbus from Prommer->UEM->UPP(MbusRx) FbusRx from Prommer->UEM->UPP FbusTx from UPP->UEM->Prommer
Cx87	"Wrong MCU ID."	RFClock UPP(Vcore)
Startup for flashing	Required startup for flashing	Vflash1 VBatt

Charging Operation

Battery

The 3125 uses a Lithium-Ion cell battery with a capacity of 850 mAh. A resistor reading inside the battery pack on the BSI line indicates the battery size. An NTC resistor close to the SIM connector measures the phone's temperature on the BTEMP line.

Temperature and capacity information are needed for charge control. These resistors are connected to the BSI pins on the UEM. The phone has 100KΩ pull-up resistors for these lines so that they can be read by A/D inputs in the phone.

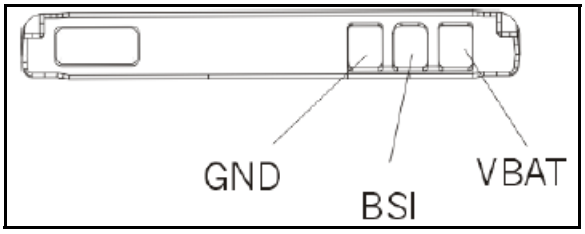


Figure 14: BL-5C battery pack pin order

Charging Circuitry

The UEM ASIC controls charging depending on the charger being used and the battery size. External components are needed for EMC, reverse polarity, and transient protection of the input to the baseband module. The charger connection is through the system connector interface. The 3125 baseband is designed to support DCT3 chargers from an electrical point of view. Both 2- and 3-wire type chargers are supported. For the 3-wire charger, the control line is not supported and not connected to the baseband ASICs.

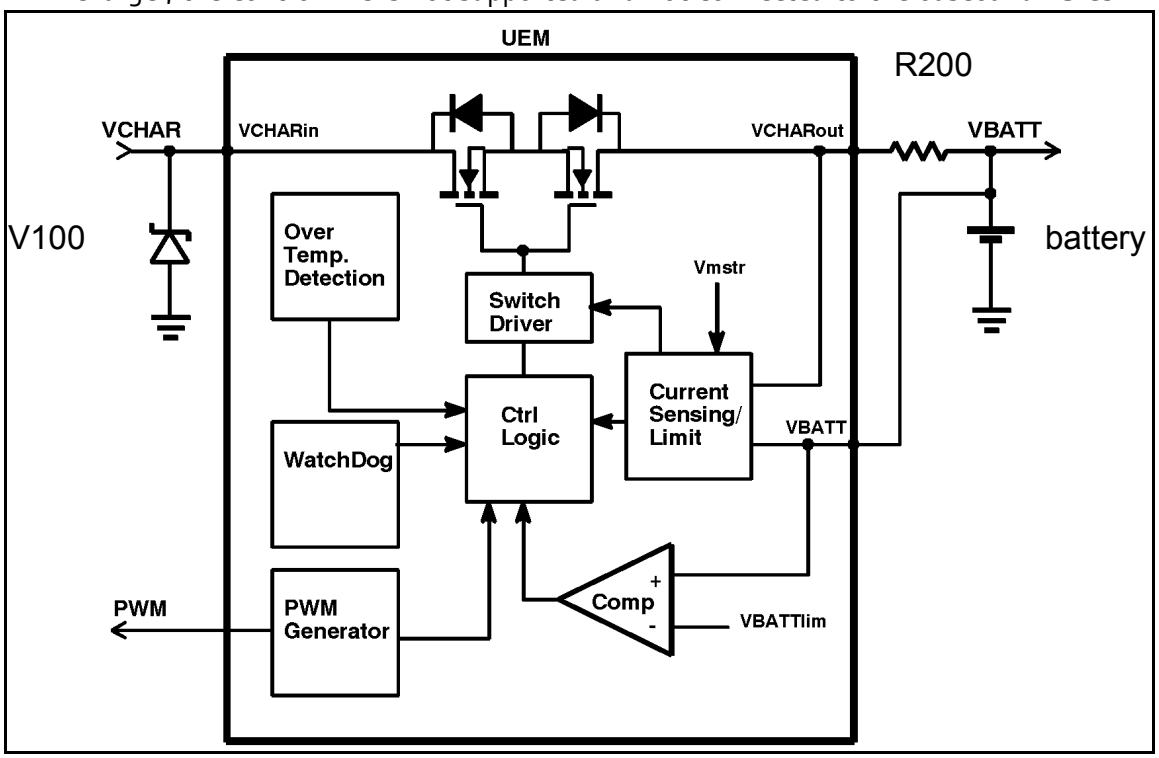


Figure 15: Charging circuitry

Charger Detection

Connecting a charger creates voltage on the VCHAR input of the UEM. Charging starts when the UEM detects the VCHAR input voltage level above 2 V (VCHdet+ threshold). The VCHARDET signal is generated to indicate the presence of the charger for the SW. The EM SW controls the charger identification/acceptance.

The charger recognition is initiated when the EM SW receives a "charger connected" interrupt. The algorithm basically consists of the following three steps:

1. Check that the charger output (voltage and current) is within safety limits
2. Identify the charger as a 2- or 3-wire charger
3. Check that the charger is within the charger window (voltage and current)

If the charger is accepted and identified, the appropriate charging algorithm is initiated.

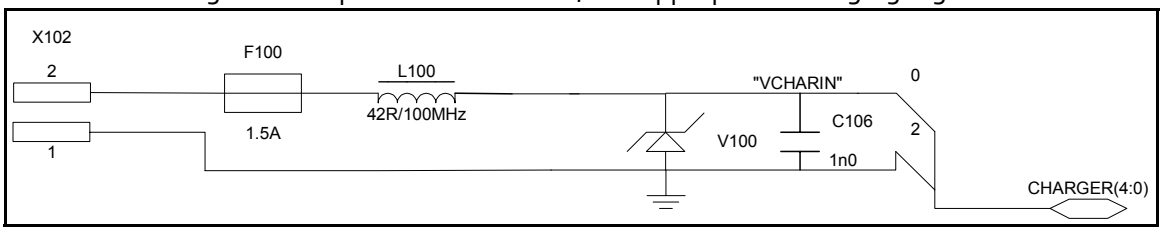


Figure 16: Charging circuit

Charge Control

In active mode, charging is controlled by the UEM's digital part. Charging voltage and current monitoring is used to limit charging into safe area. For this reason, the UEM has the following programmable charge cut-off limits:

- VBATLim1=3.6 V (Default)
- VBATLim2L=5.0 V
- VBATLim2H=5.25 V

VBATLim1, 2L, 2H are designed with hystereses. When the voltage rises above VBATLim1, 2L, 2H+ charging is stopped by turning the charging switch off. No change is done in operational mode. After the voltage has decreased below VBATLim-, charging restarts.

There are two PWM frequencies in use depending on the type of the charger. A 2-wire charger uses a 1 Hz, while a 3-wire charger uses a 32Hz. The duty cycle range is 0% to 100%. The maximum charging current is limited to 1.2 A.

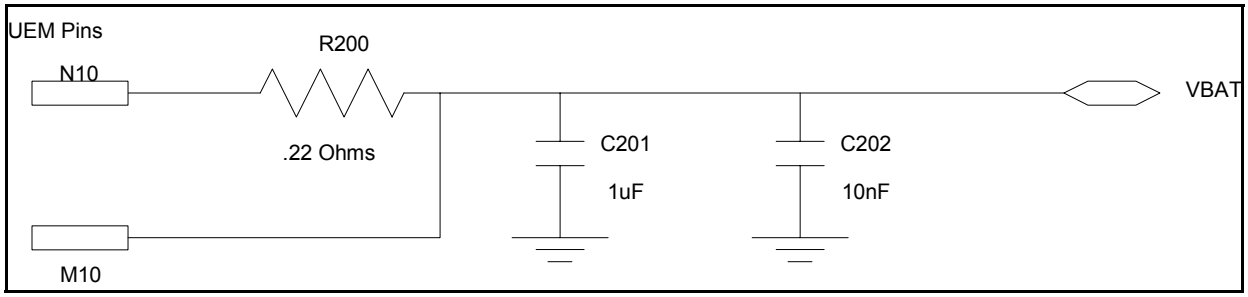


Figure 17: Charging circuity at the battery

Audio

The audio control and processing in the 3125 is provided by the UEM, which contains the audio codec, and the UPP, which contains the MCU and DSP blocks. These blocks handle and process the audio data signals.

The baseband supports three microphone inputs and two earpiece outputs. The microphone inputs are MIC1, MIC2, and MIC3. MIC1 input is used for the phone's internal microphone; MIC2 input is used for headsets (HDB-4). MIC3 is not used. Every microphone input can have either a differential or single-ended AC connection to UEM circuit. In 3125 (RH-61), the internal microphone (MIC1) and external microphone (MIC2) for Pop-Port™ accessory detection are both differential. The microphone signals from different sources are connected to separate inputs at the UEM. Inputs for the microphone signals are differential types. Also, MICBIAS1 is used for MIC1 and MICBIAS2 is used for MIC2.

Display and Keyboard

The 3125 uses LEDs for the color LCD and keypad illumination. There are two LEDs for the LCD and four LEDs for the keypad. KLIGHT is the signal used to drive the LED driver for the LCD and keyboard. This signal turns on the LED driver. The interface uses a 9-bit data transfer and is quite similar to the DCT3 type interface, except the Command/Data information is transferred together with the data.

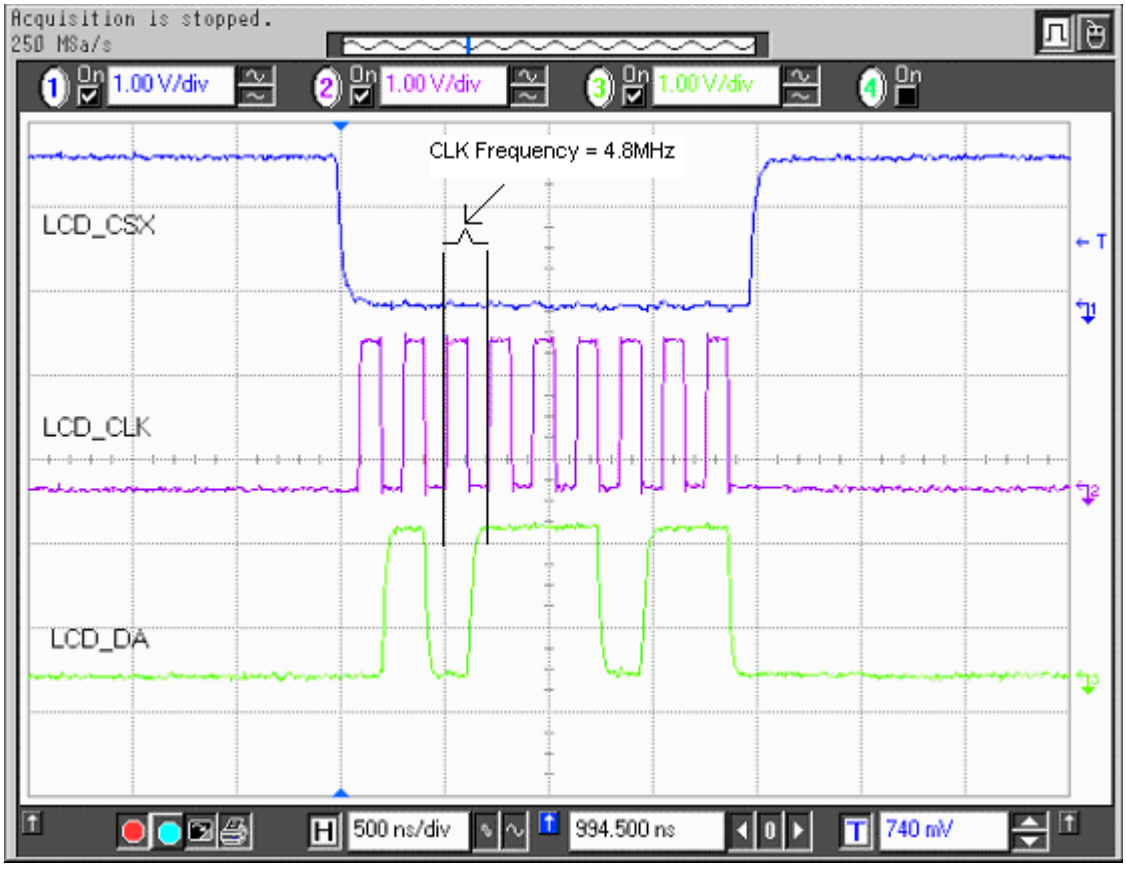


Figure 18: Waveform for the LCD Interface

Accessories

The 3125 supports Pop-Port and Universal Headset accessories, differential and single-ended, respectively. Detection of the Pop-Port accessories is done through the ACI signal where the Universal Headset is detected on GenIO (12).

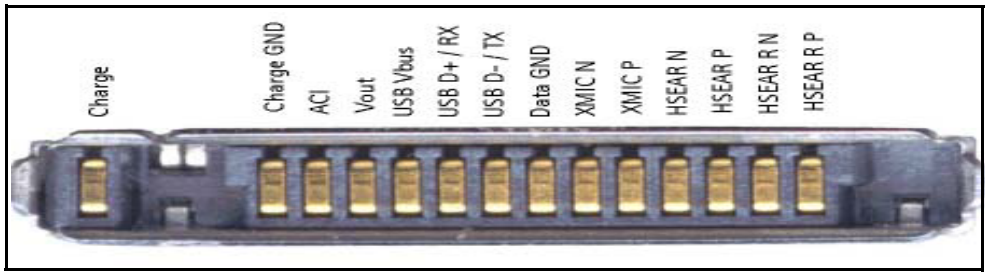


Figure 19: Pop-Port connector pin out

The pin out on the Pop-Port connector is as follows:

- Charger
- Charger GND
- ACI
- Vout
- USB Vbus
- USB D+ / Fbus Rx
- USB D- / Fbus Tx
- Data GND
- XMic N
- XMic P
- HSear N
- HSear P
- HSear R N
- HSear R P

You can perform the following in Pop-Port accessories:

- Charging
- Accessory detection
- FBUS communication
- USB communication
- Fully differential audio interface for mono- and stereo outputs

Charging

Charging through Pop-Port is accomplished in the same manner as through the charger connector. Pin 1 of the Pop-Port is physically connected to the charger connector. When the phone is connected to a desktop charger (e.g., DCV-15), it charges in the same manner as it does with the charger connector.

Figure 20 shows the actual charging sequence. The channels on the diagram are:

- CH1 = Charging current across the .22 Ohm (R200) resistor on UEMK
- CH2 = Charger voltage measure at V100
- CH3 = Battery voltage measure at R200
- CH4 = PURX

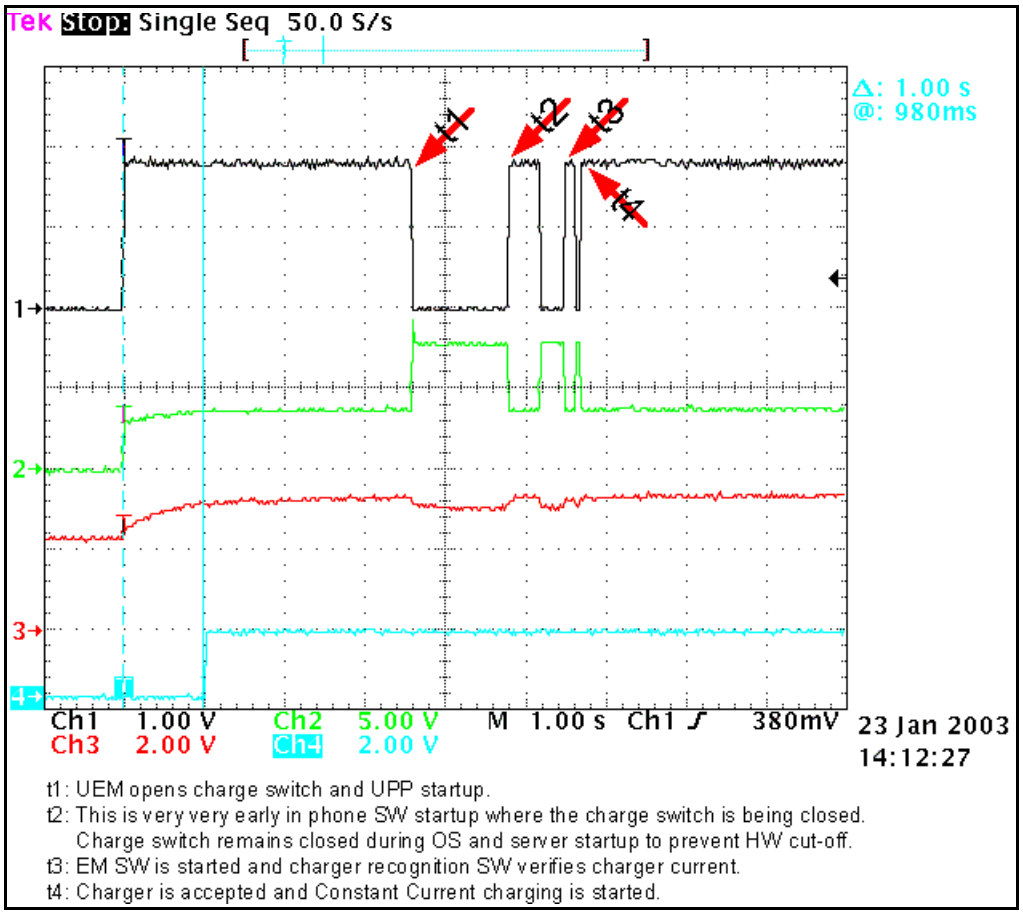


Figure 20: Charging sequence

In Channel 4, PURX is released, which indicates when the phone operation goes from RESET mode to POWER ON mode.

Pop-Port Headset Detection

Accessory detection on the Pop-Port is done digitally. The pins used for this accessory detection are:

- Pin 2 (Charge GND)
- Pin 3 (ACI)
- Pin 4 (Vout)

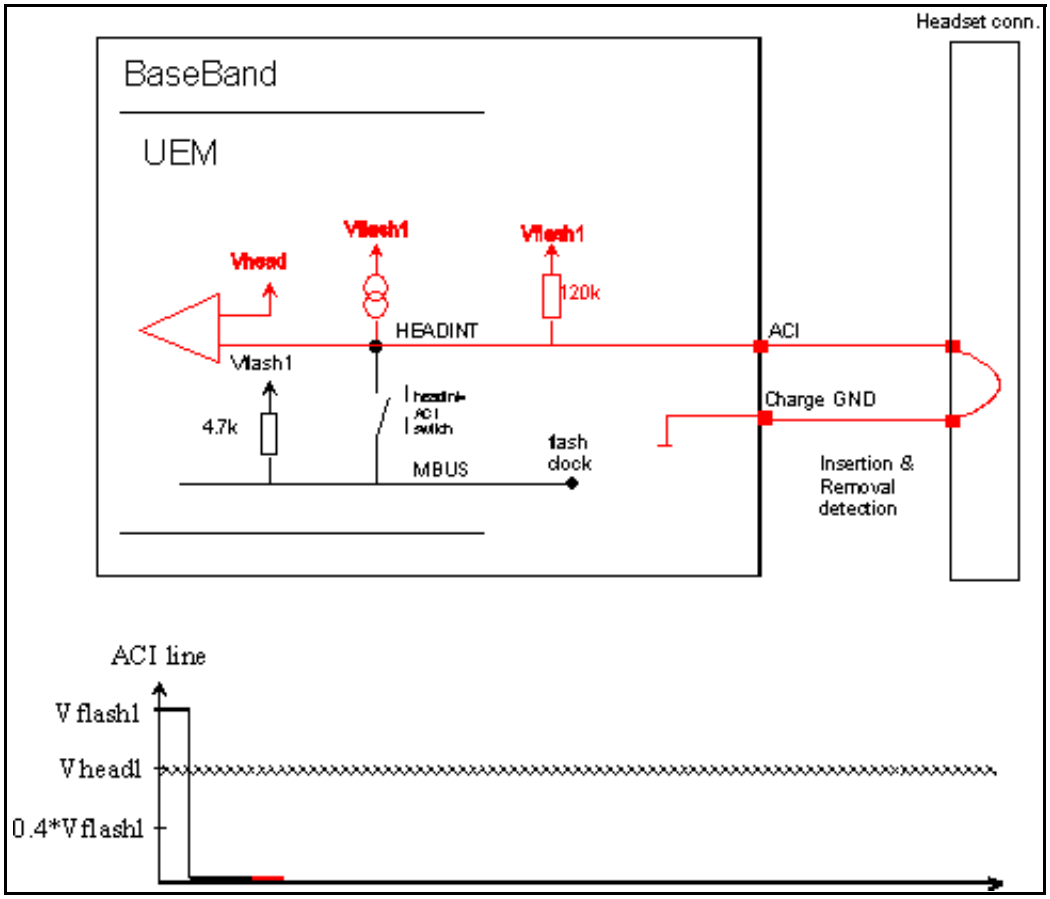


Figure 21: Waveform showing Pop-Port accessory detection

FBus Detection

FBus communication in Pop-Port is done through the following lines:

- Pin 2 (Charge GND)
- Pin 3 (ACI)
- Pin 4 (Vout)
- Pin 6 (FBus Rx)
- Pin 7 (FBus Tx)

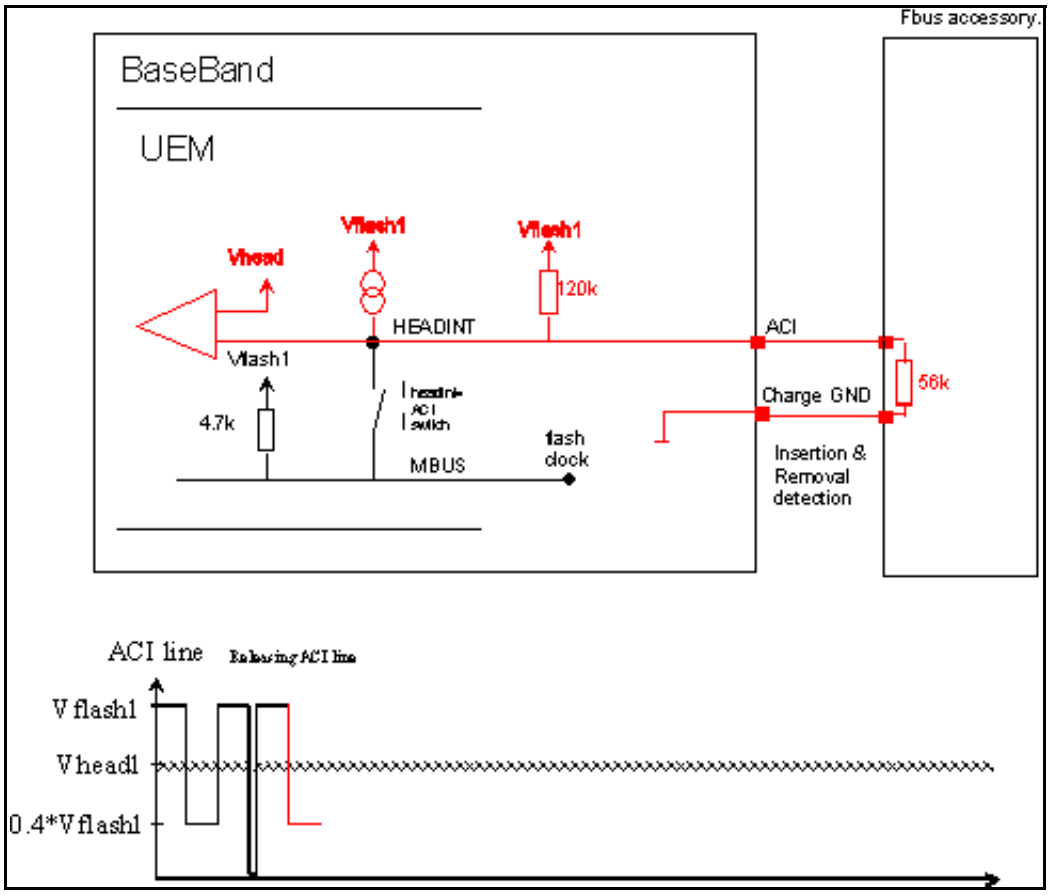


Figure 22: Waveform showing Pop-Port FBus communication

Accessory Detection Through ACI

USB and Audio on (mono or stereo)/FM radio communication in Pop-Port is done through the following signals:

Table 4: Accessory Detection Signals

USB	Audio/FM
Pin 5 (USB Vbus)	Pin 9 (XMic N)
Pin 6 (USB +)	Pin 10 (SMIC P)
Pin 7 (USB -)	Pin 11 (HSEAR N)
Pin 8 (Data GND)	Pin 12 (HSEAR P)

Table 4: Accessory Detection Signals (Continued)

USB	Audio/FM
	Pin 13 (HSEAR R N)
	Pin 14 (HSEAR R P)

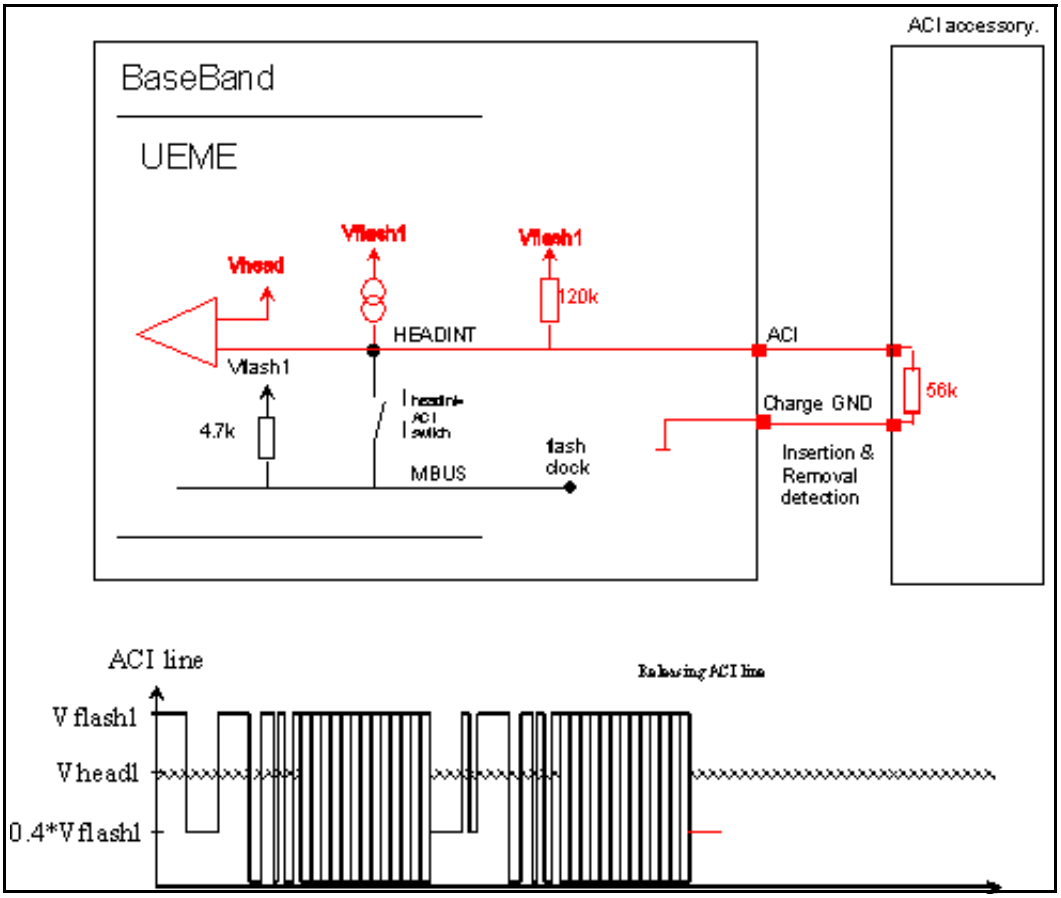


Figure 23: Waveform showing accessory detection through ACI

SIM CAR

The 3125 supports SIM CAR. Use the waveform in Figure 24 to verify that the sim_vcc, sim_i/o, cim_clk, and sim_rst signals are activated in the correct sequence at power up. This picture may be taken when the SIM CAR is installed on the phone to measure the signals when the phone is turned on. The figure shows the proper waveforms when the interface is working. See Figure 27 on page 32 for the test point locations.

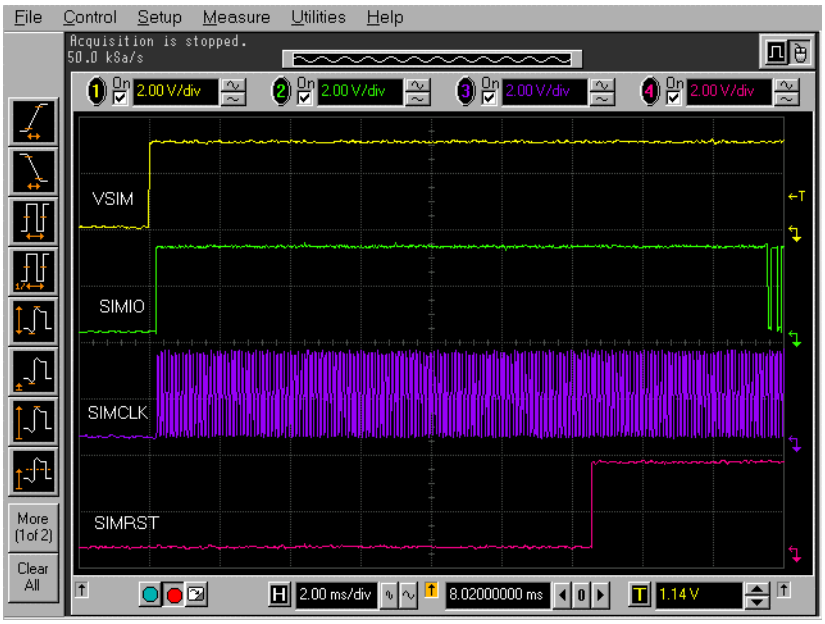


Figure 24: RUIM signal waveform

Test Points

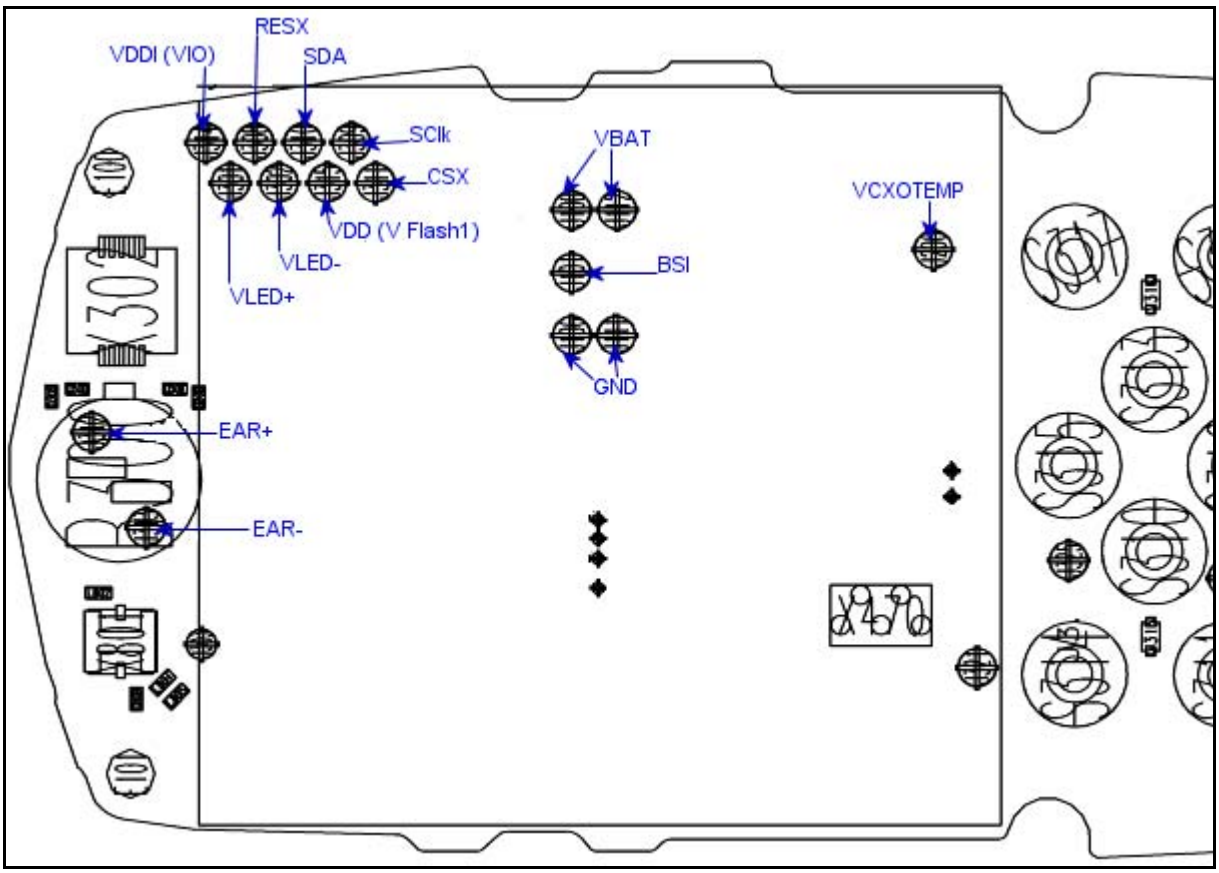


Figure 25: BB test points - Top side

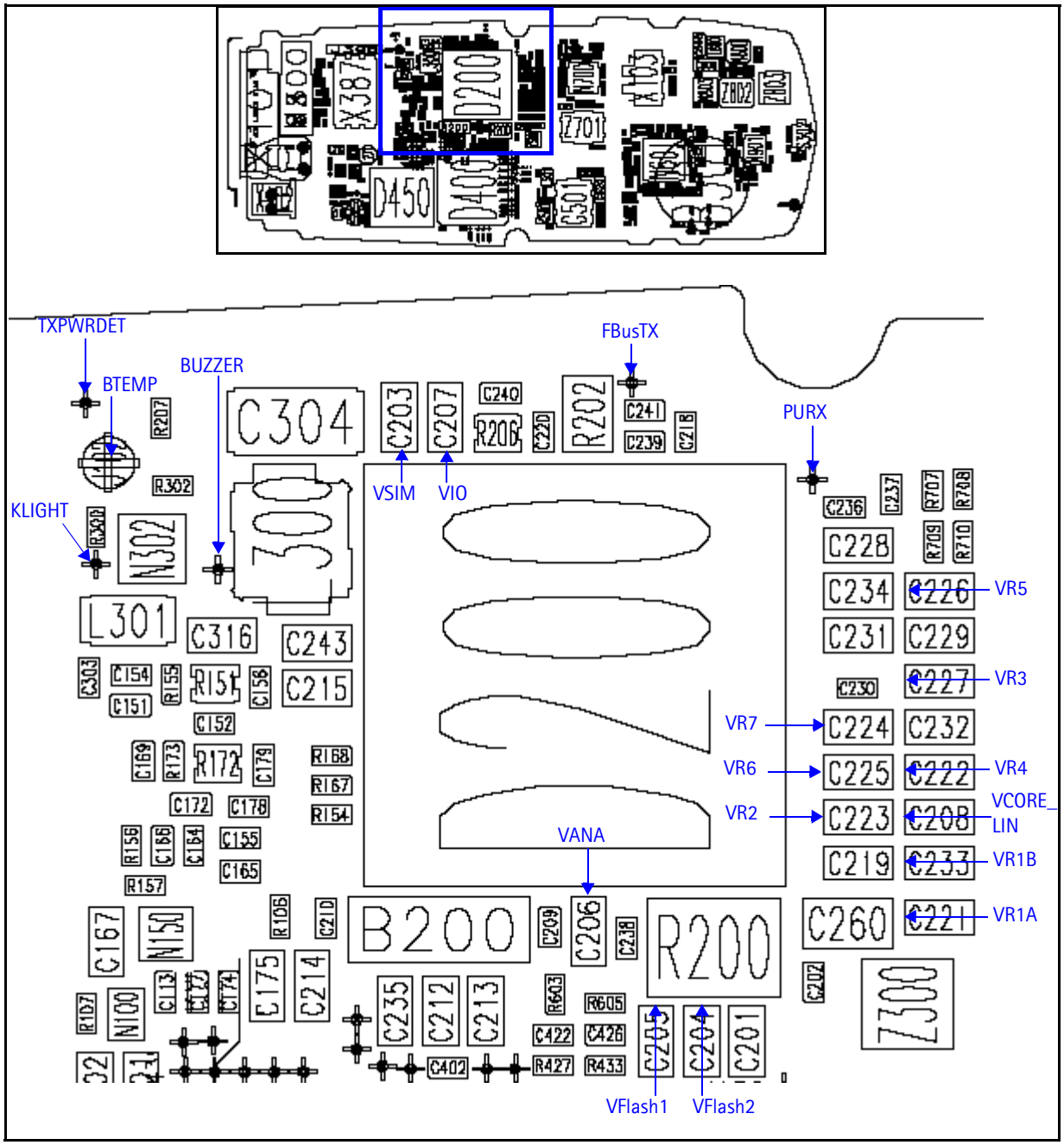


Figure 26: BB test points – Bottom side 1

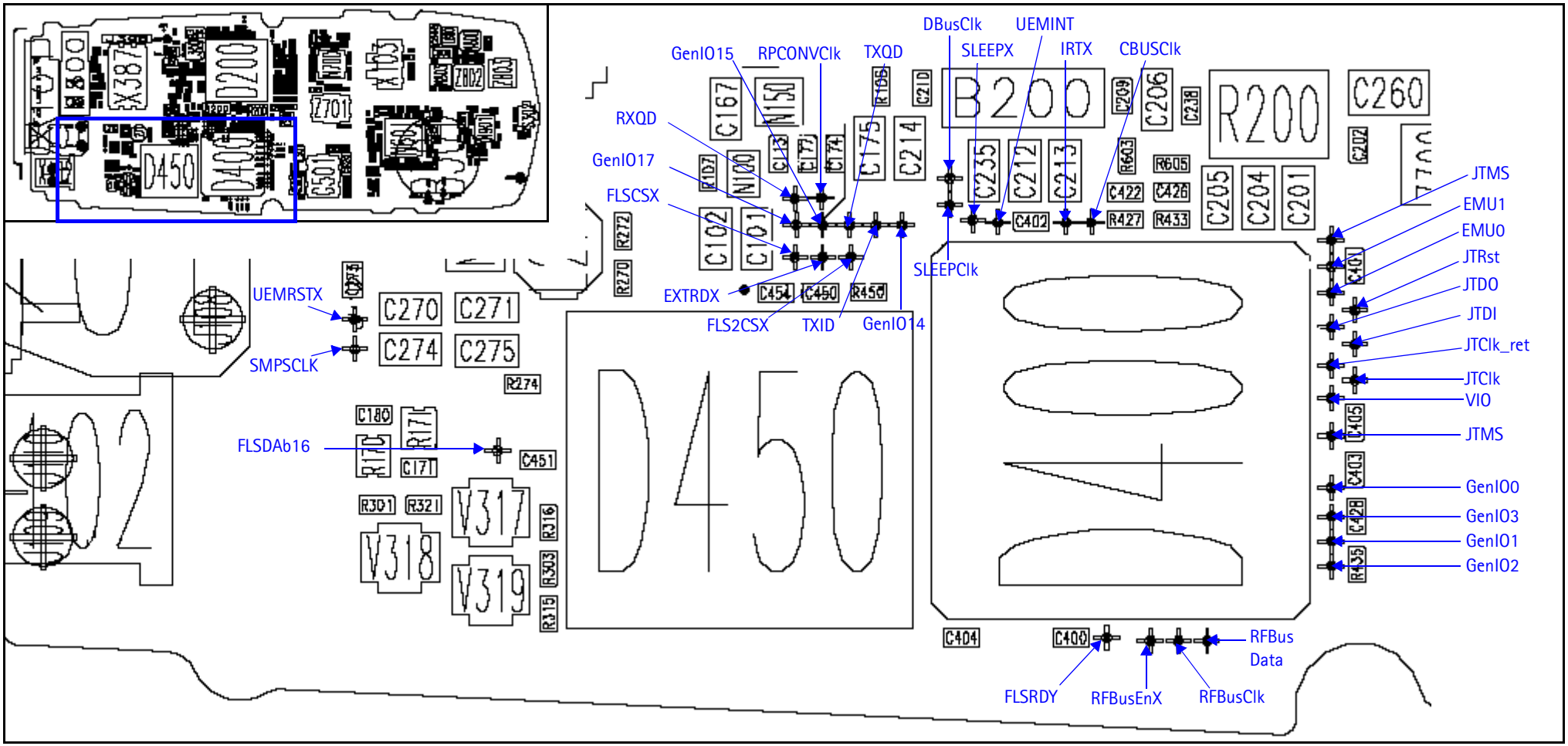


Figure 27: BB test points - Bottom side 2

Troubleshooting

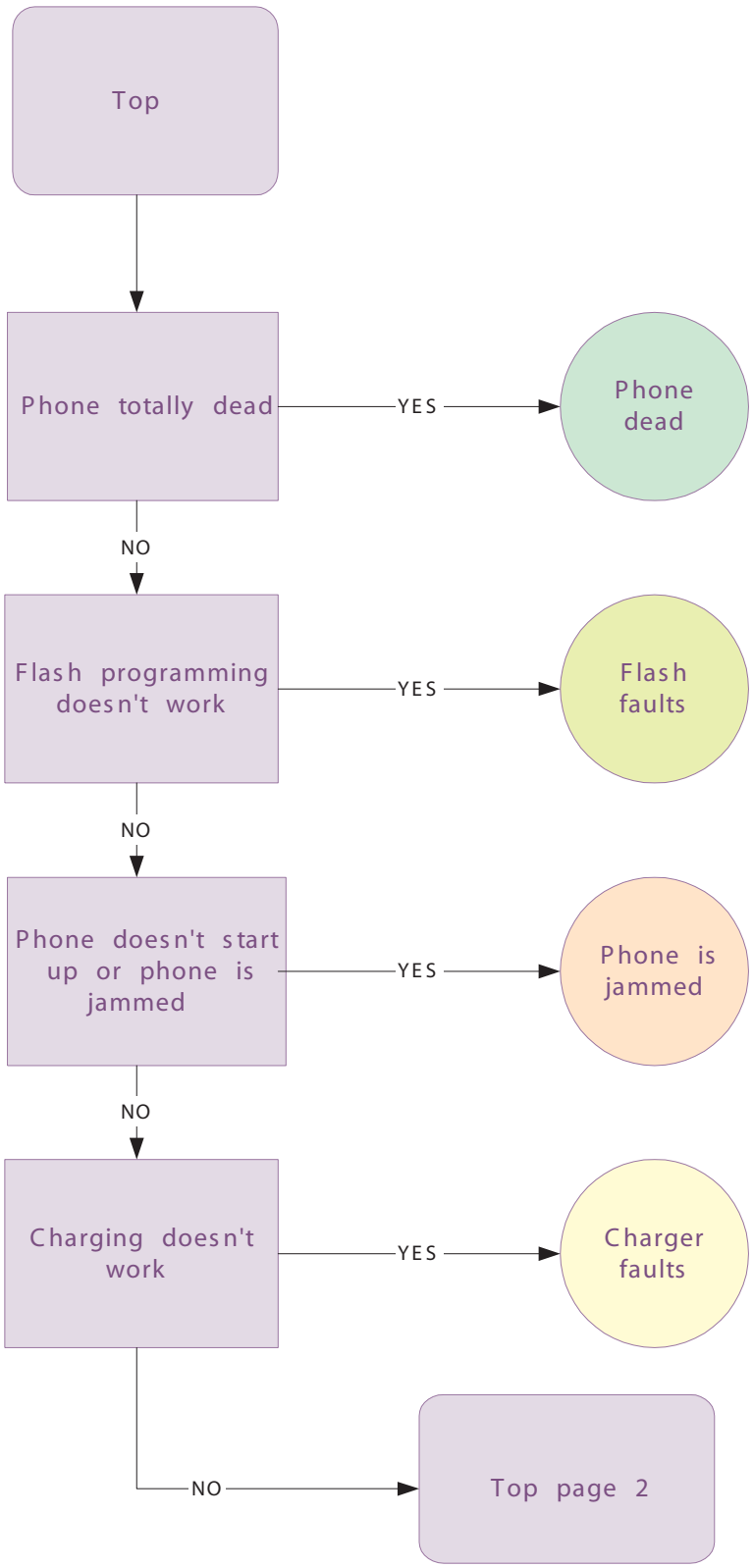
The following hints should help finding the cause of the problem when the circuitry seems to be faulty. Troubleshooting instructions are divided into the following sections:

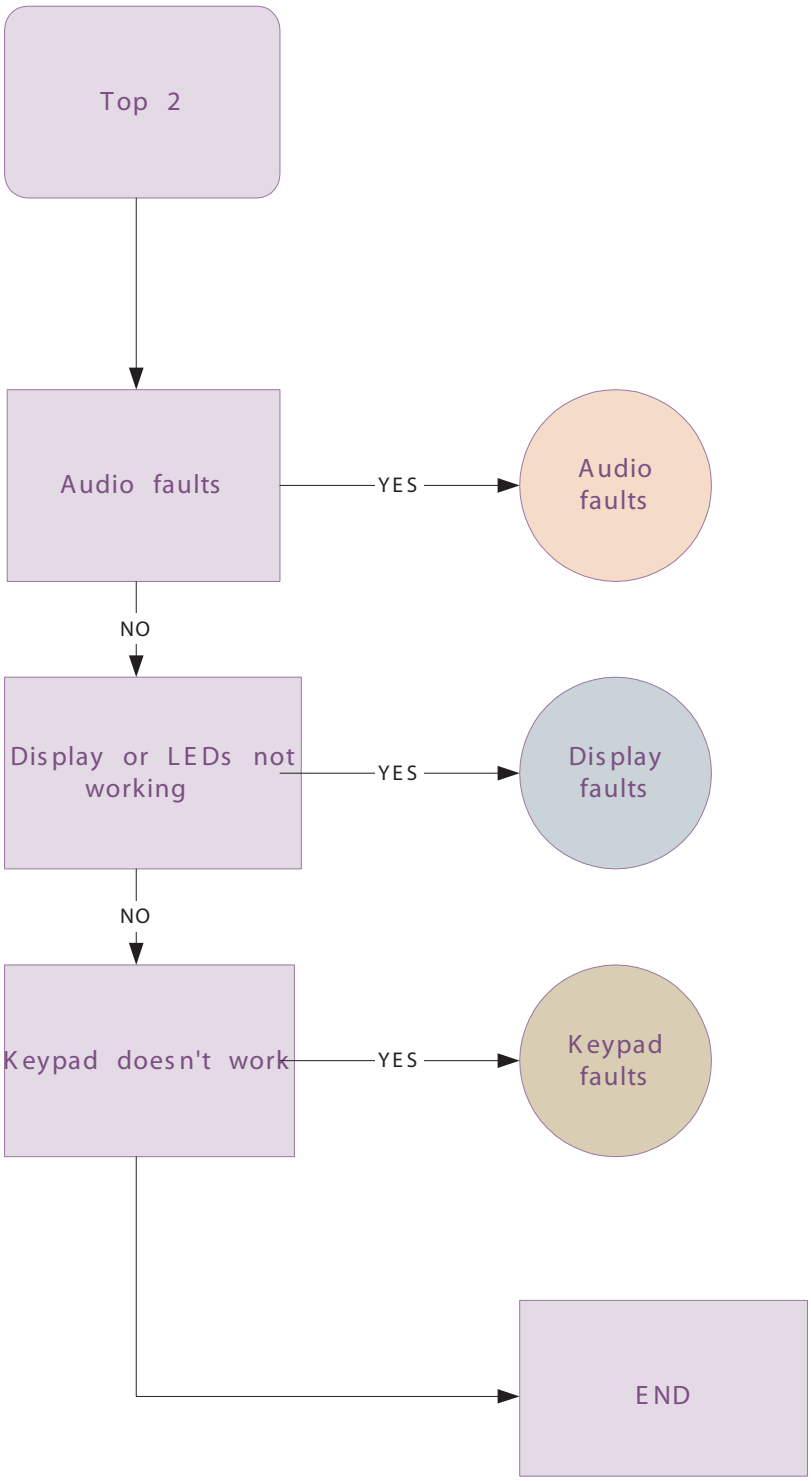
- Top troubleshooting map
- Phone is totally dead
- Power does not stay on or the phone is jammed
- Flash programming does not work
- Display is not working
- Audio fault
- Charging fault

First, carry out a thorough visual check of the module and ensure that:

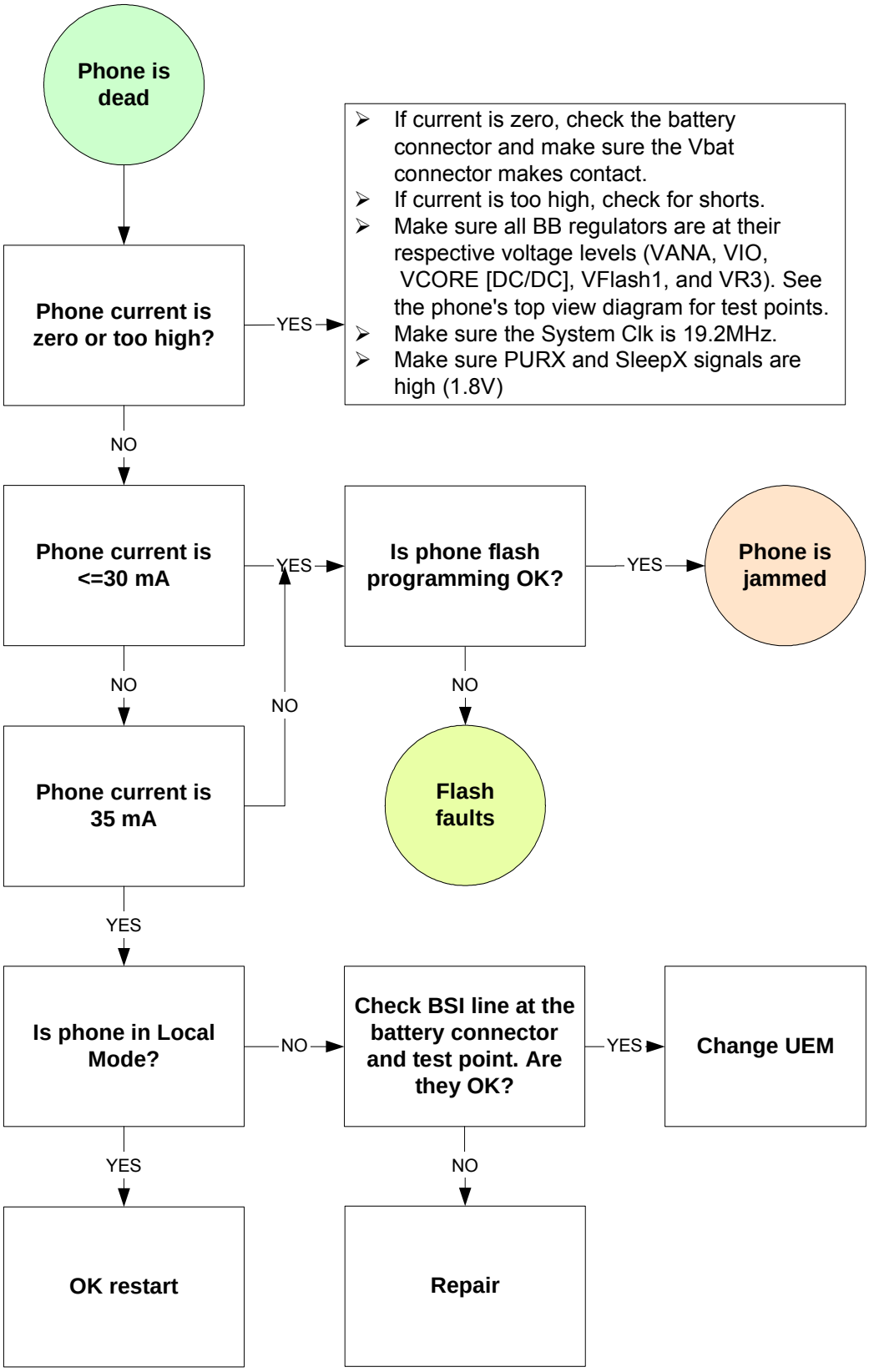
- There are no mechanical damages
- Soldered joints are OK
- ASIC orientations are OK

Top Troubleshooting Map

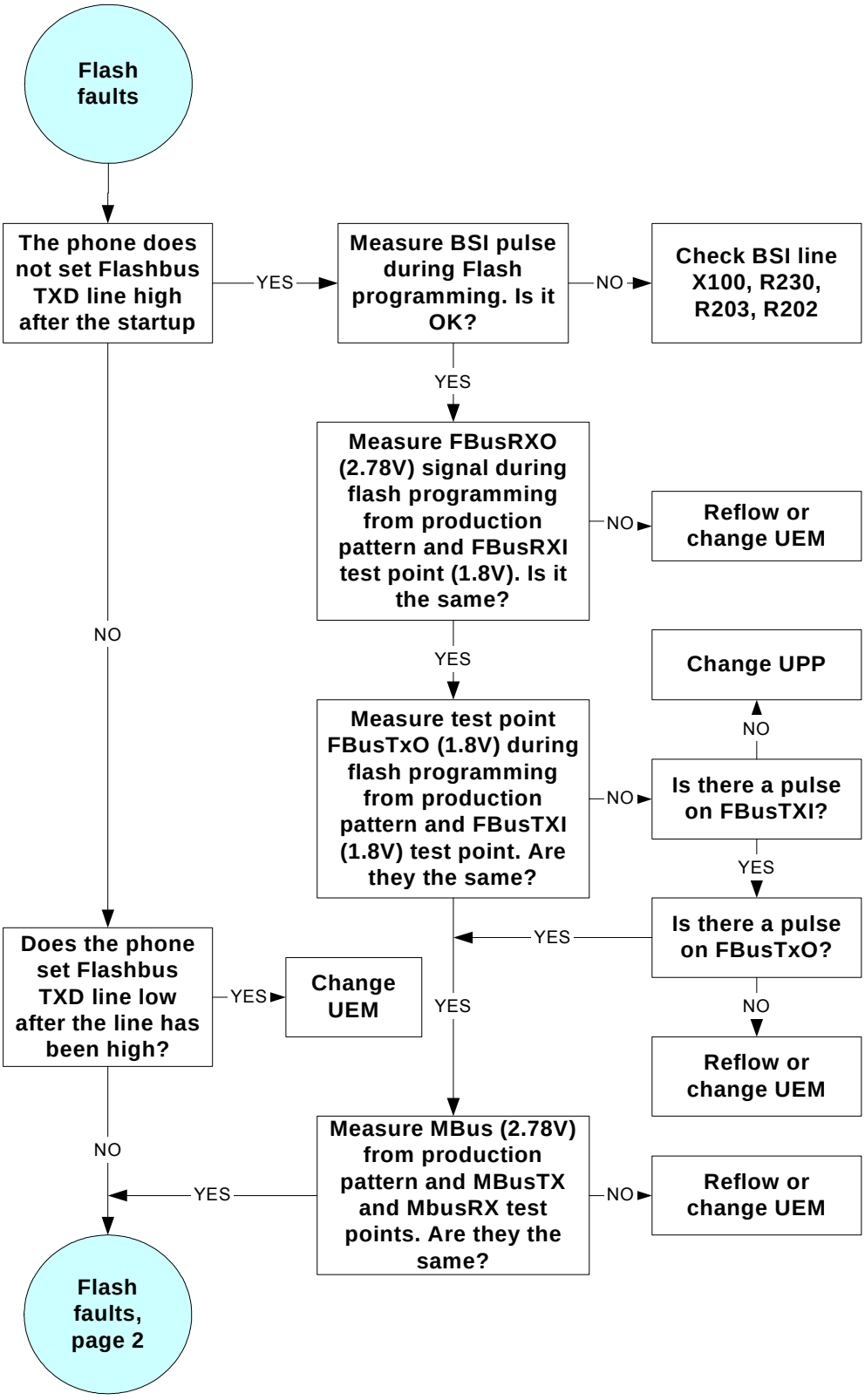


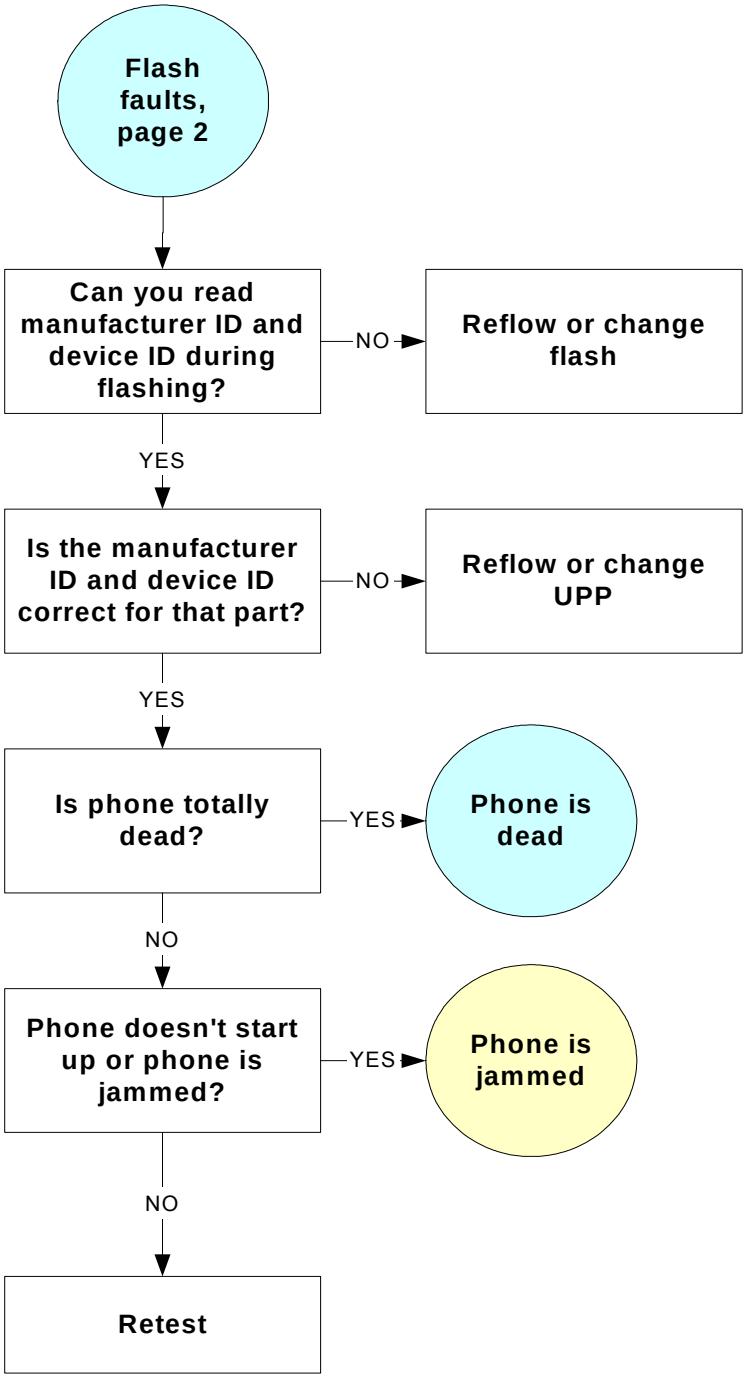


Phone is Totally Dead

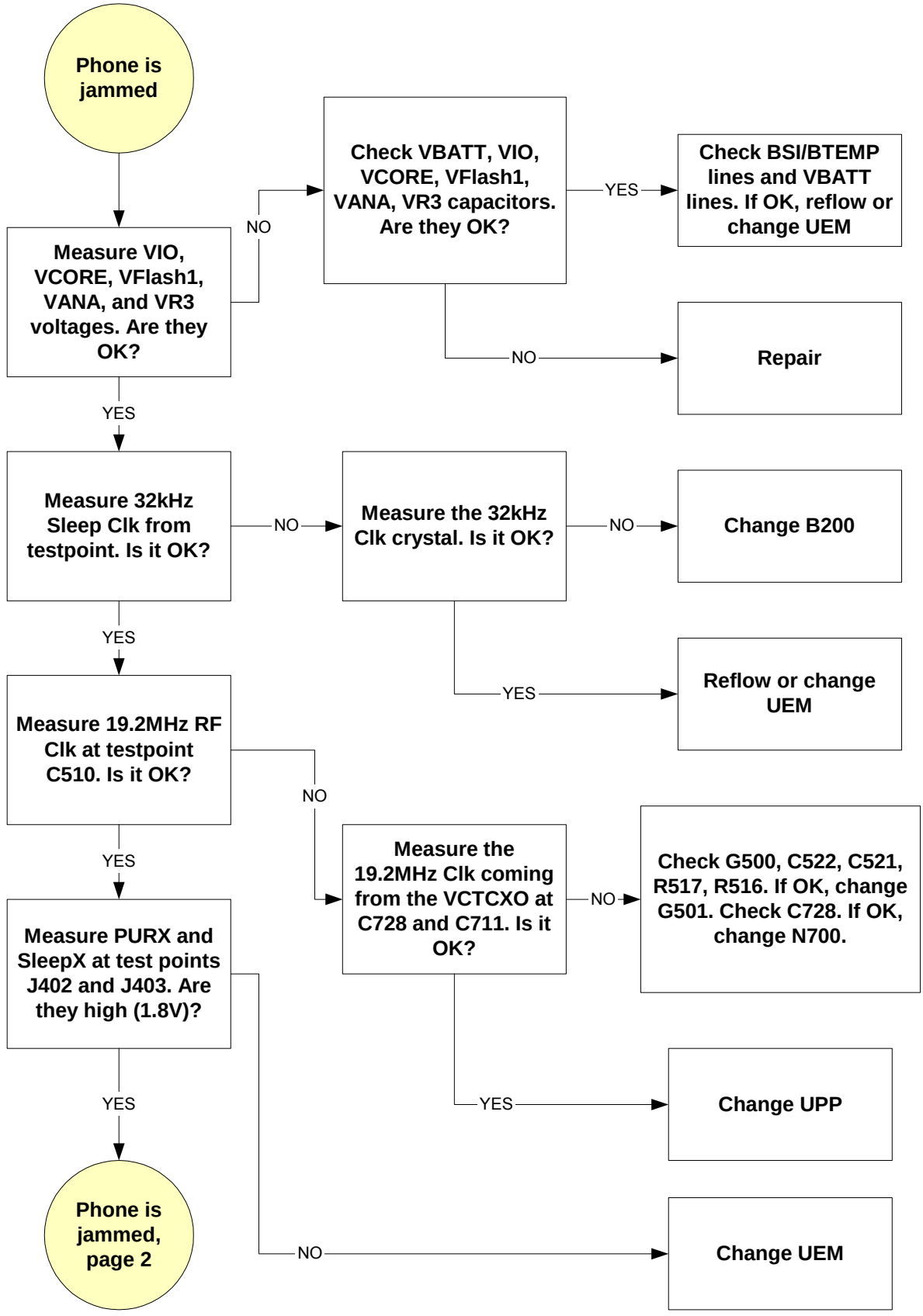


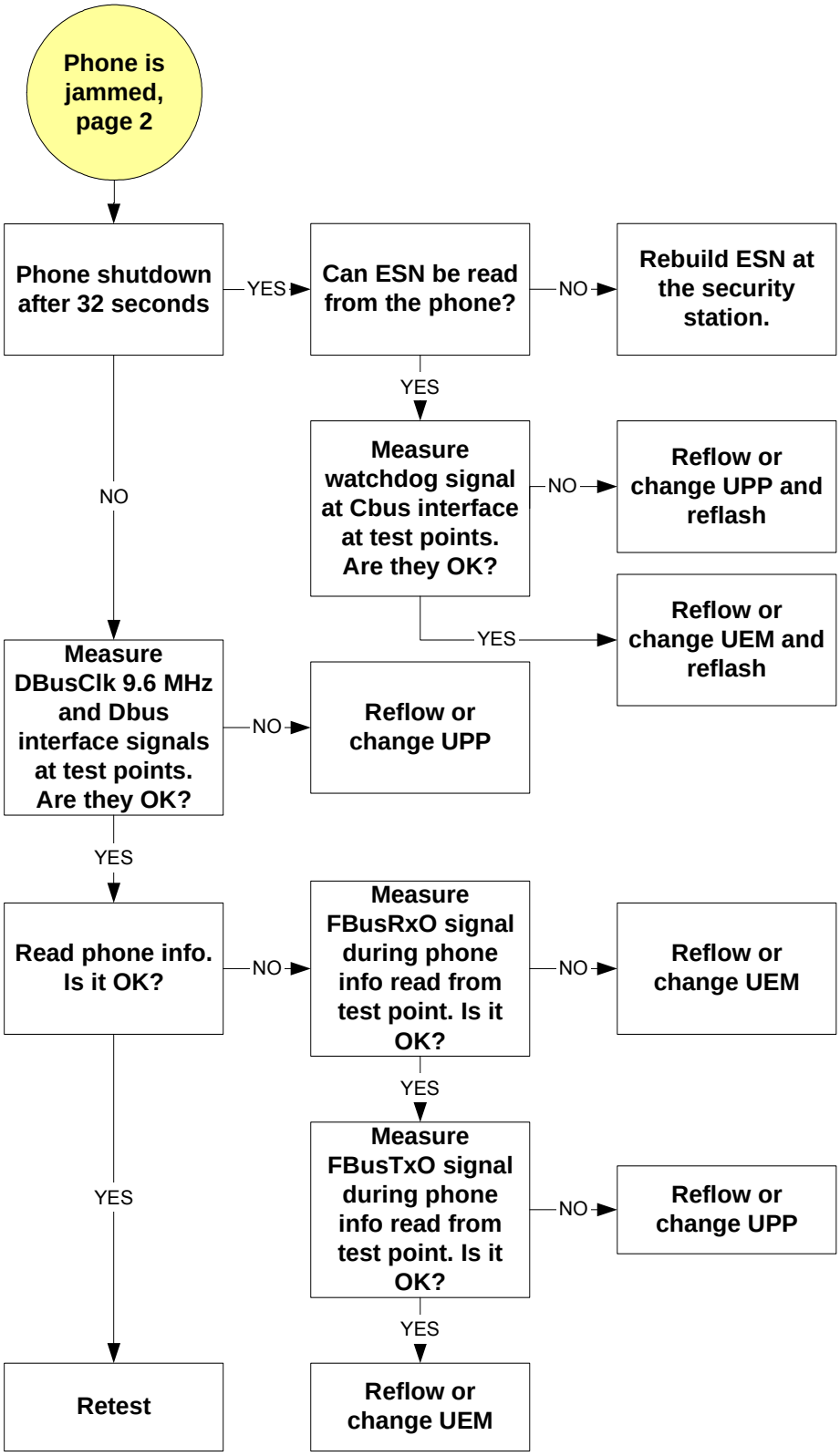
Flash Programming Does Not Work



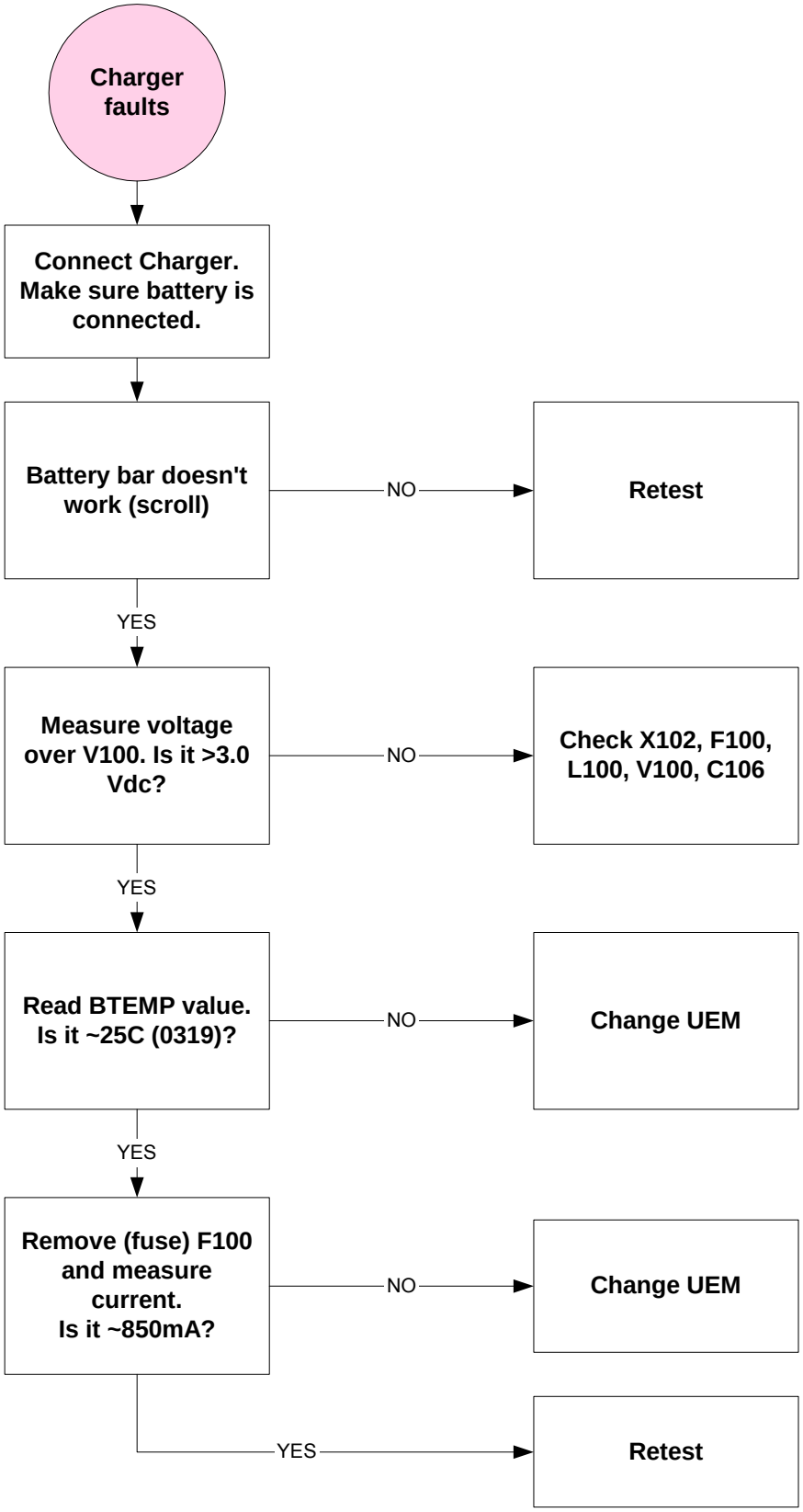


Power Does Not Stay on or the Phone is Jammed

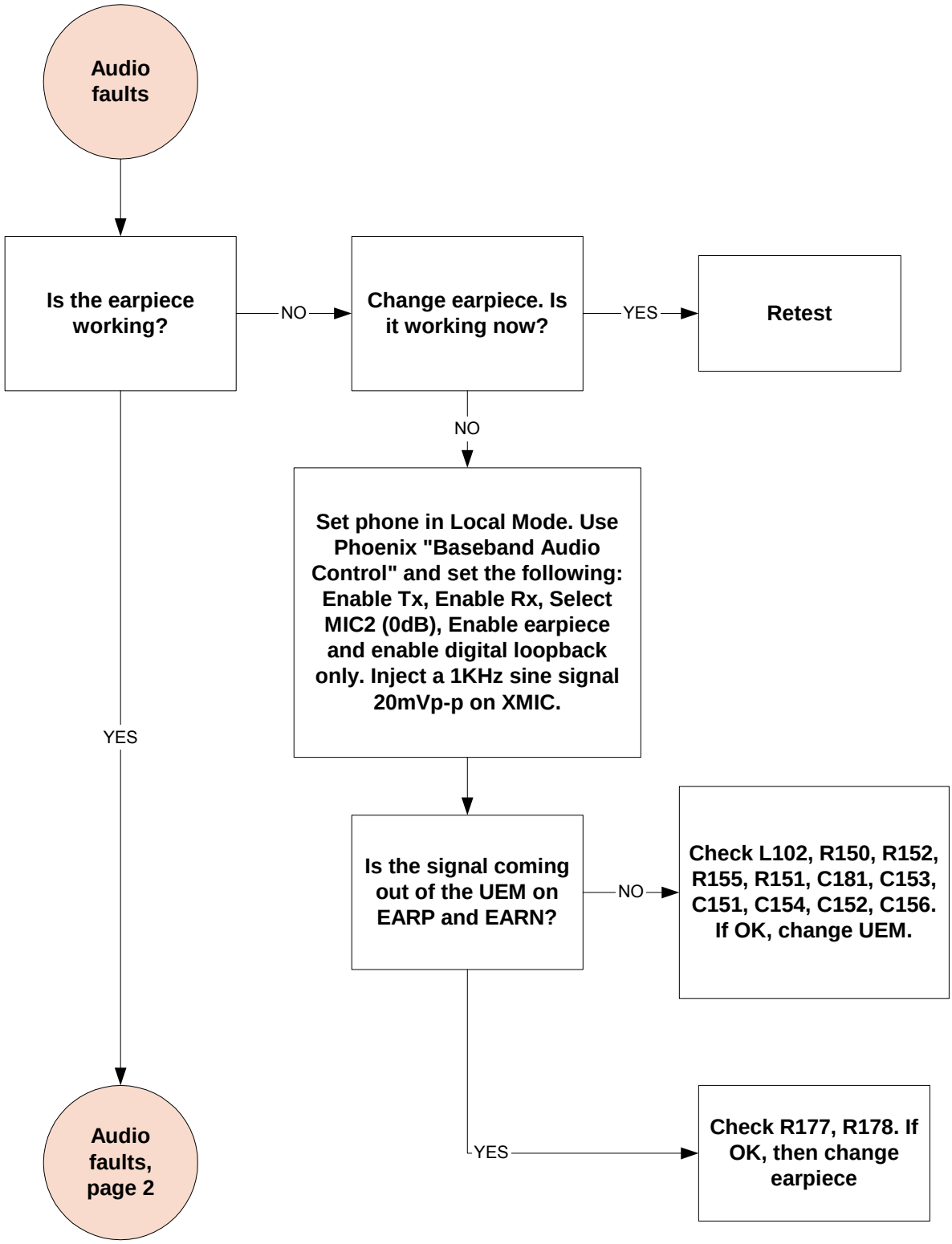


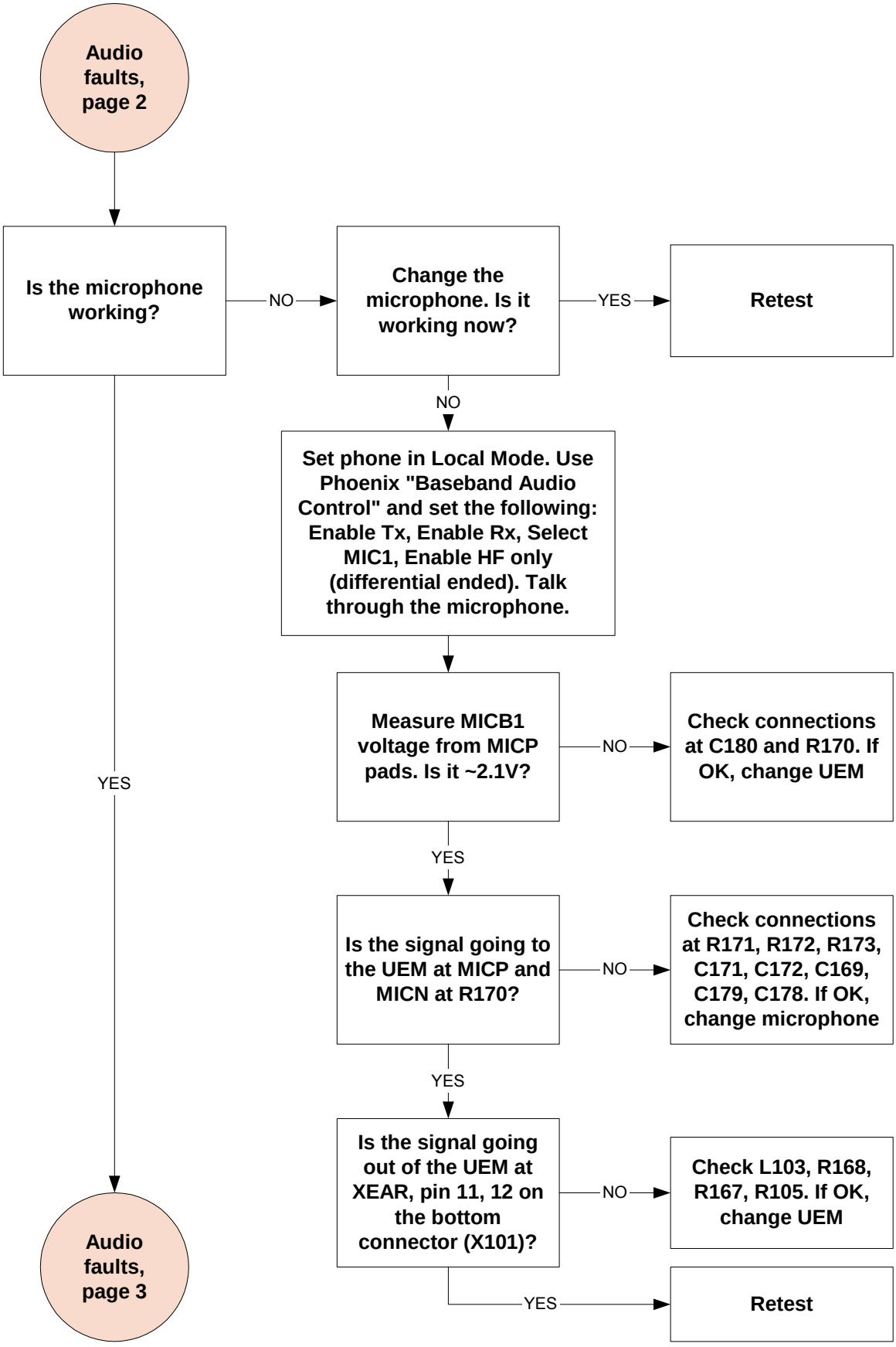

Phone is jammed, page 2
Phone shutdown after 32 seconds
YES
Can ESN be read from the phone?
NO
Rebuild ESN at the security station.
YES
Measure watchdog signal at Cbus interface at test points. Are they OK?
NO
Reflow or change UPP and reflash
YES
Reflow or change UEM and reflash
NO
Measure DBusClk 9.6 MHz and Dbus interface signals at test points. Are they OK?
NO
Reflow or change UPP
YES
Read phone info. Is it OK?
NO
Measure FBusRxO signal during phone info read from test point. Is it OK?
NO
Reflow or change UEM
YES
Measure FBusTxO signal during phone info read from test point. Is it OK?
NO
Reflow or change UPP
YES
Reflow or change UEM
YES
Retest

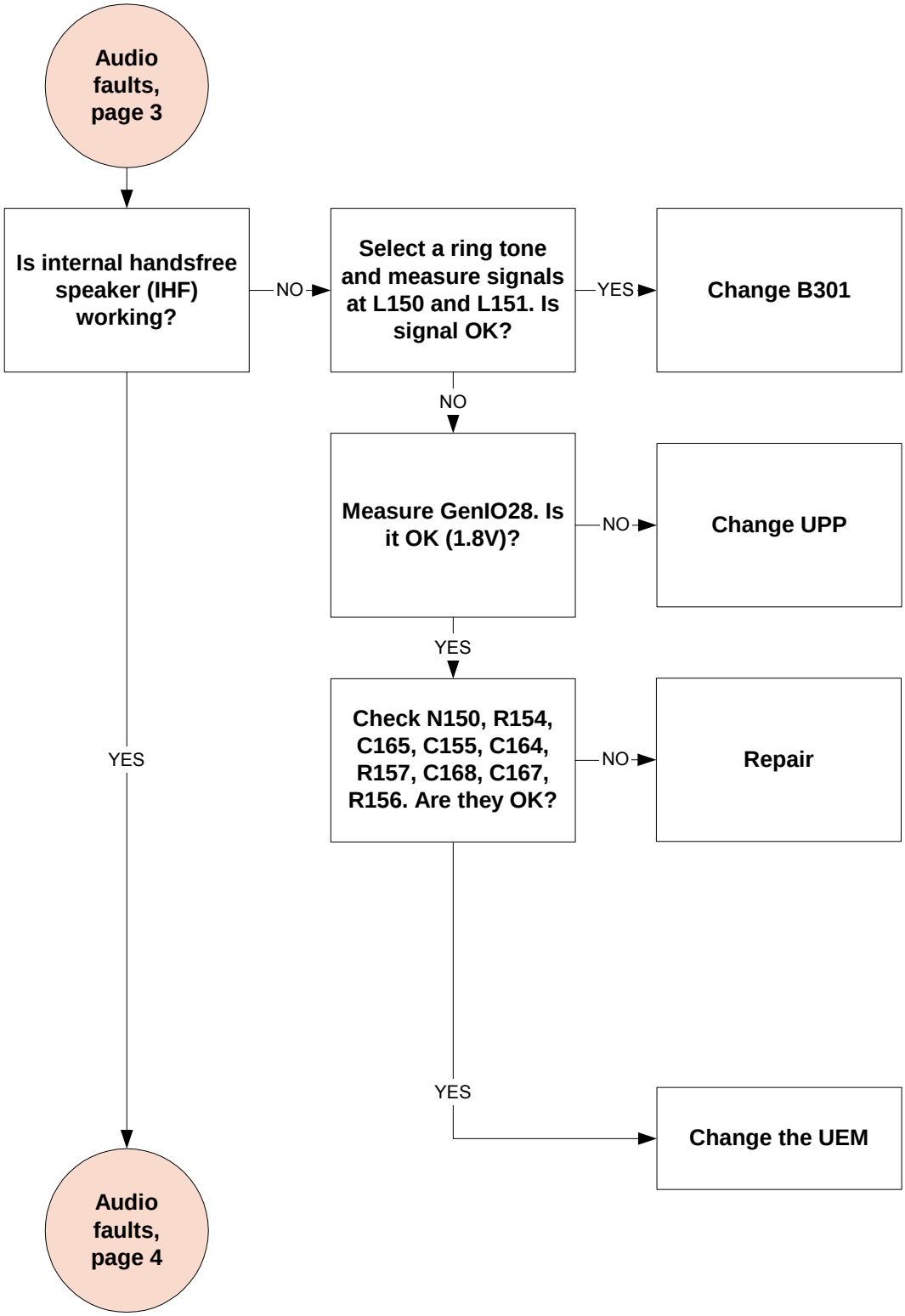
Charger

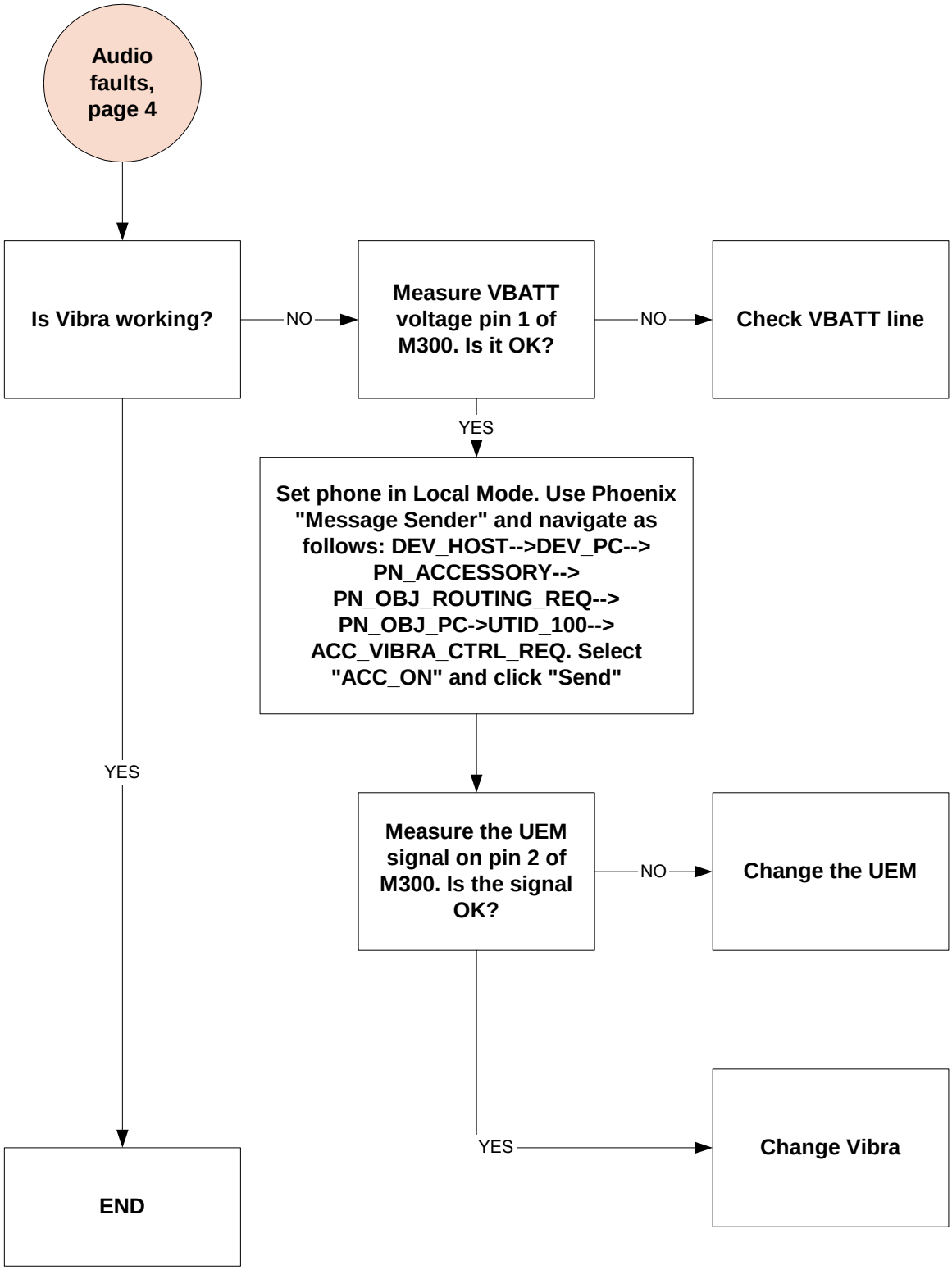

Charger faults
Connect Charger. Make sure battery is connected.
Battery bar doesn't work (scroll)
NO
Retest
YES
Measure voltage over V100. Is it >3.0 Vdc?
NO
Check X102, F100, L100, V100, C106
YES
Read BTEMP value. Is it ~25C (0319)?
NO
Change UEM
YES
Remove (fuse) F100 and measure current. Is it ~850mA?
NO
Change UEM
YES
Retest

Audio Faults

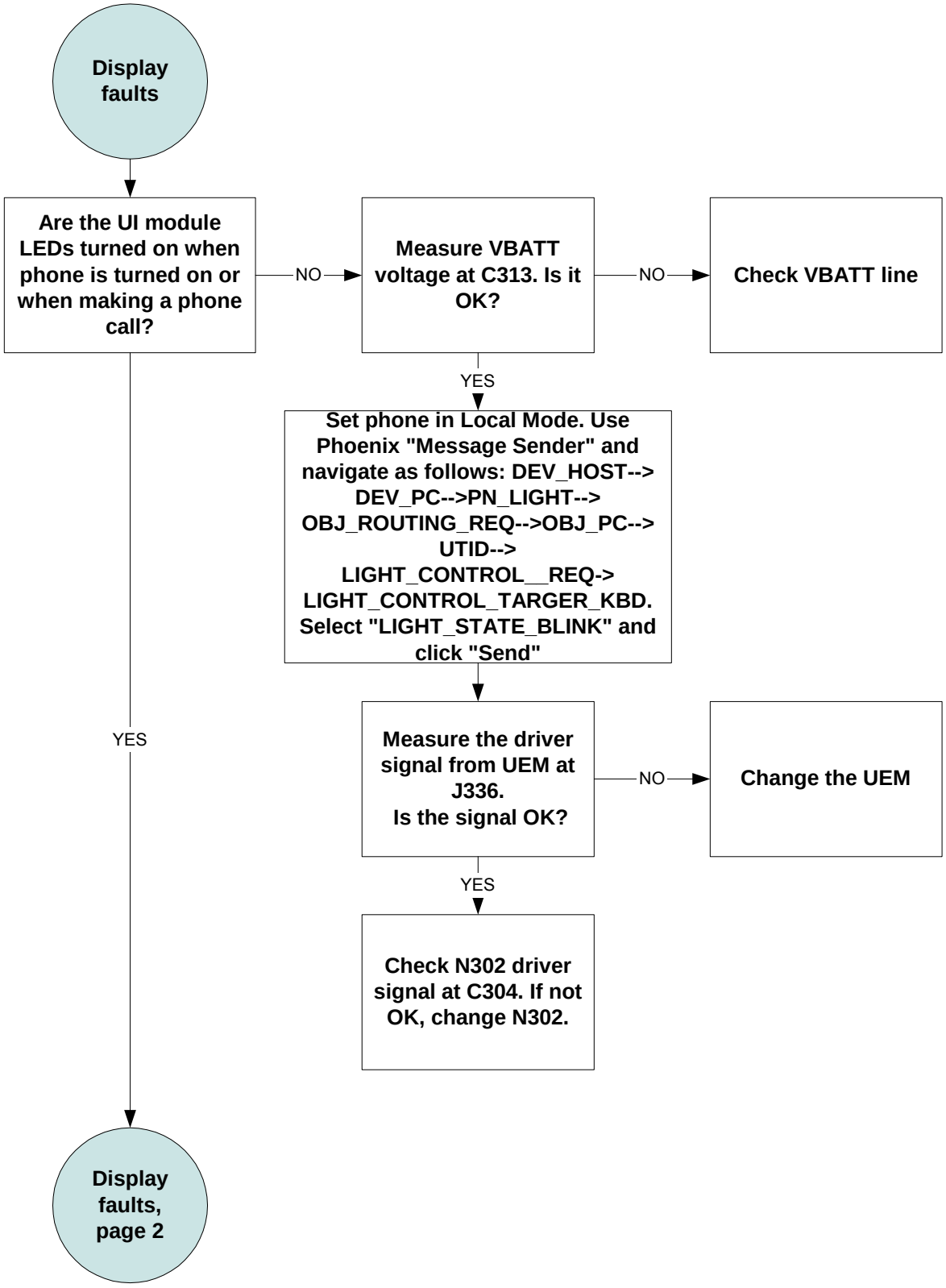


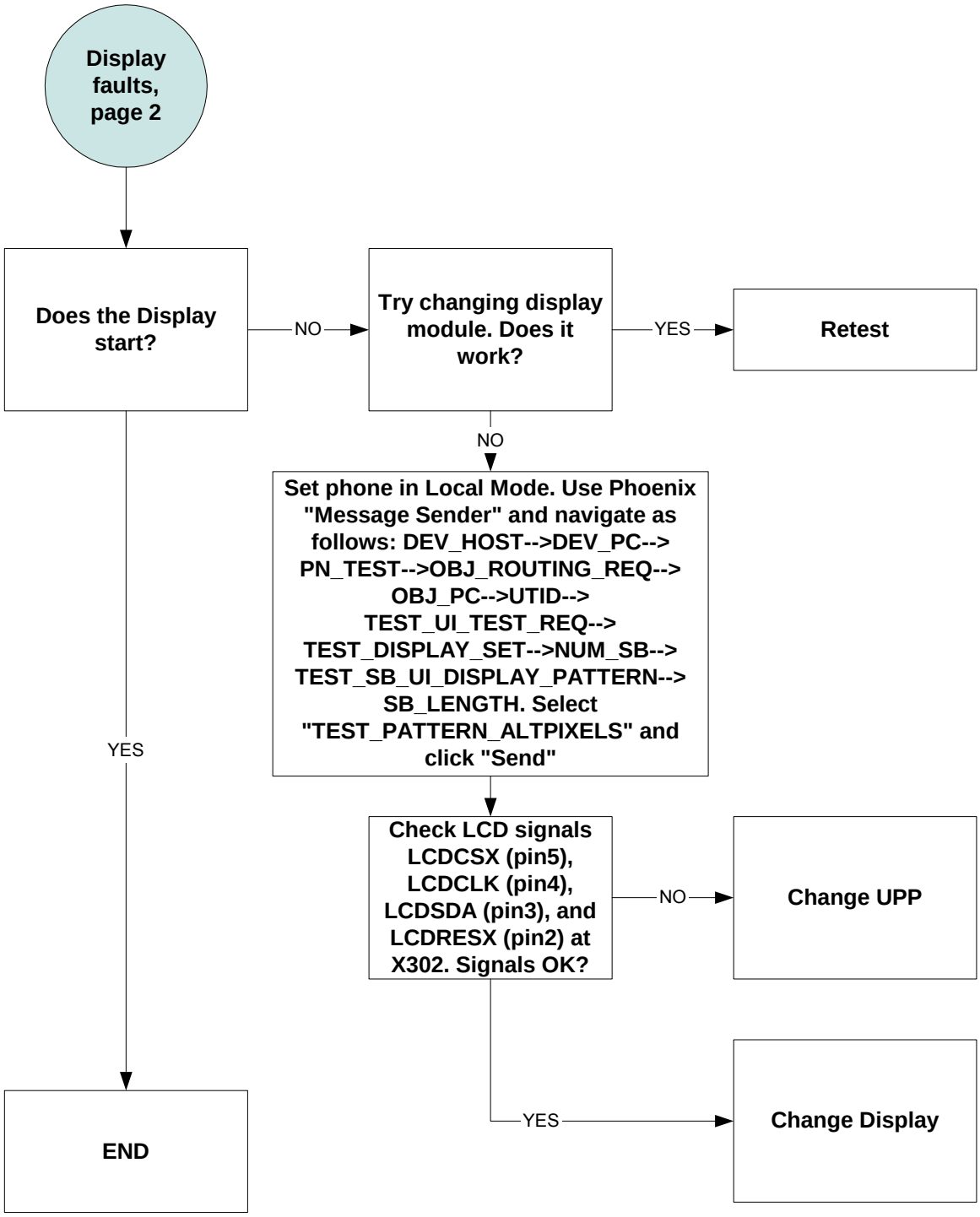




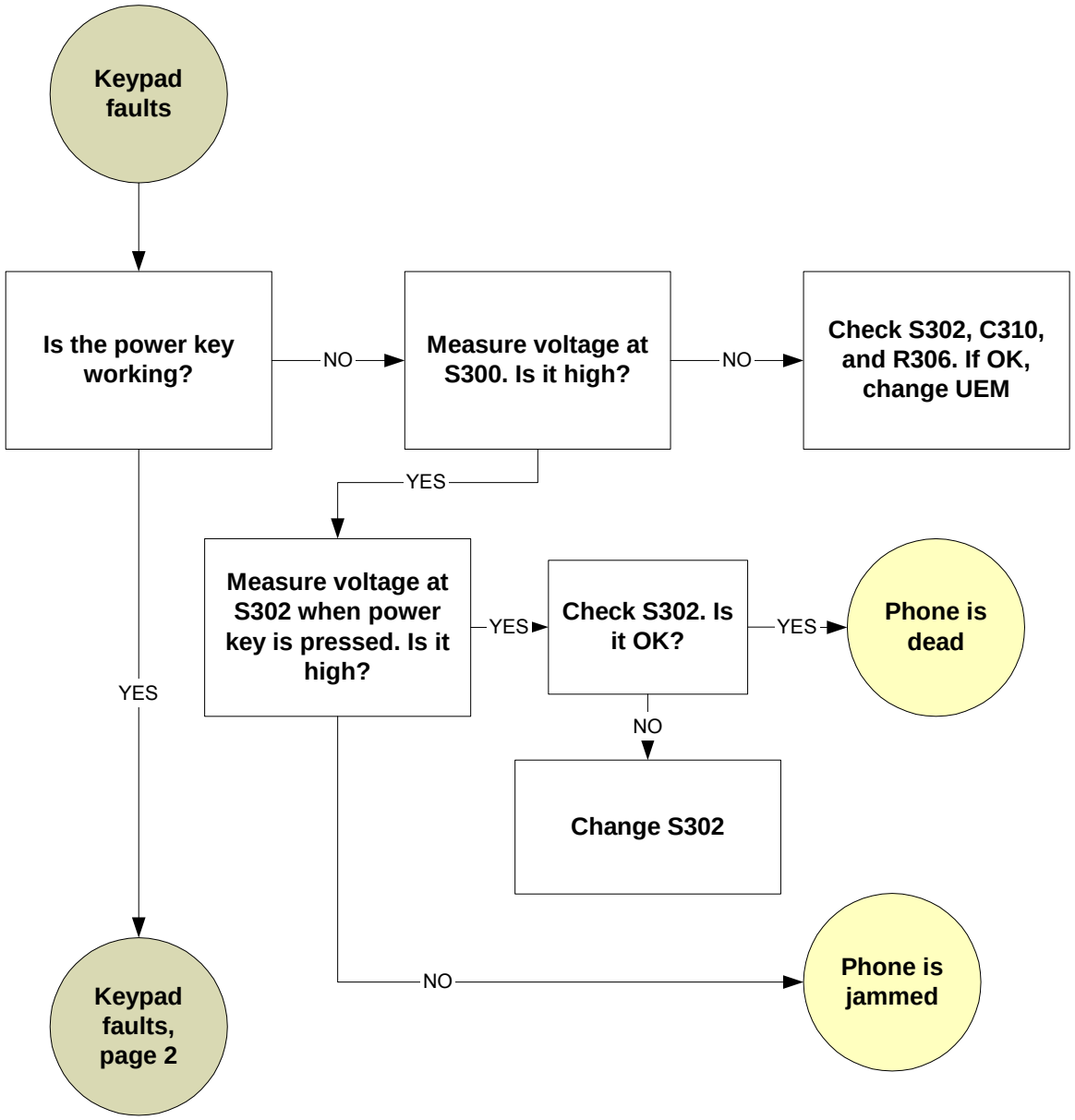


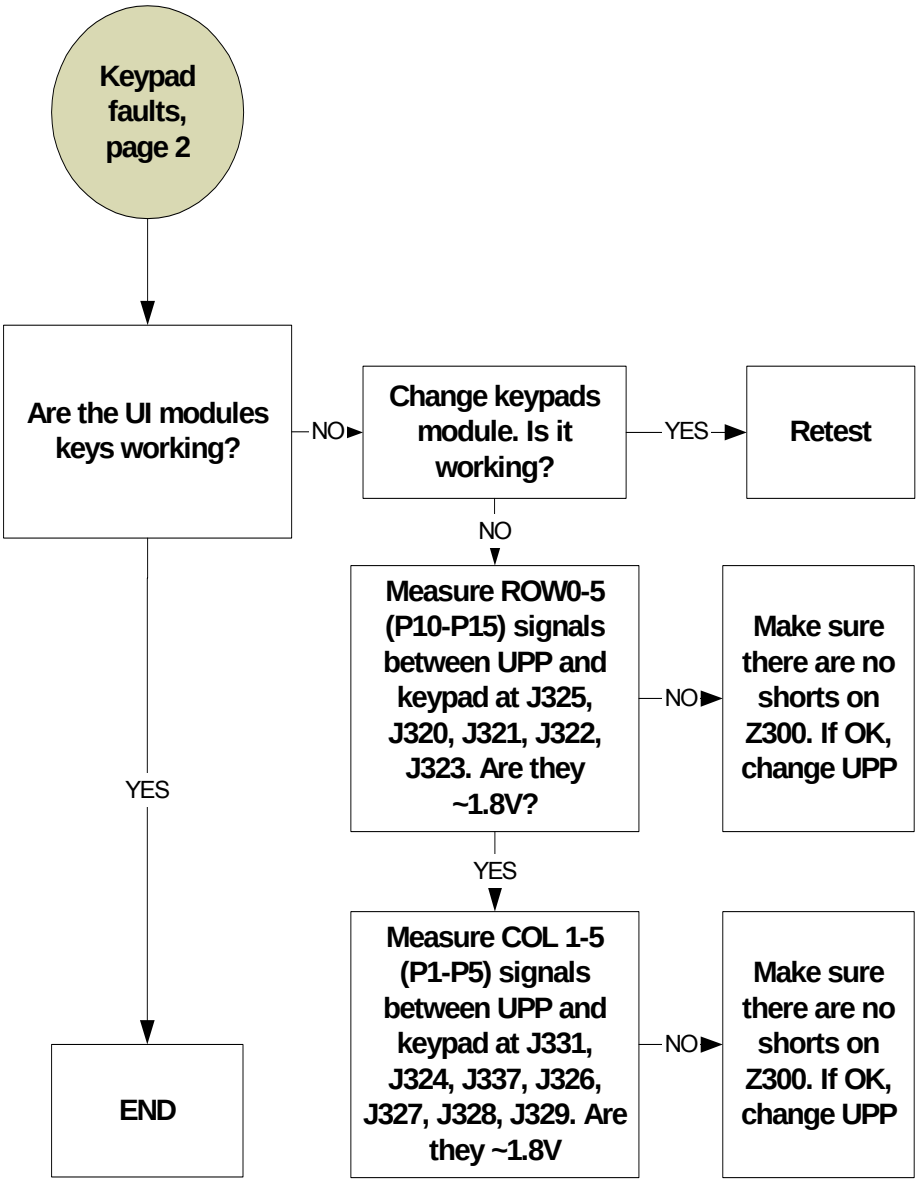
Display Faults




Display faults, page 2
Does the Display start?
NO
Try changing display module. Does it work?
YES
Retest
NO
Set phone in Local Mode. Use Phoenix "Message Sender" and navigate as follows: DEV_HOST-->DEV_PC--> PN_TEST-->OBJ_ROUTING_REQ--> OBJ_PC-->UTID--> TEST_UI_TEST_REQ--> TEST_DISPLAY_SET-->NUM_SB--> TEST_SB_UI_DISPLAY_PATTERN--> SB_LENGTH. Select "TEST_PATTERN_ALTPIXELS" and click "Send"
YES
Check LCD signals LCDCSX (pin5), LCDCLK (pin4), LCDSDA (pin3), and LCDRESX (pin2) at X302. Signals OK?
NO
Change UPP
YES
Change Display
END

Keypad Faults




Keypad faults, page 2
Are the UI modules keys working?
NO
Change keypads module. Is it working?
YES
Retest
NO
Measure ROW0-5 (P10-P15) signals between UPP and keypad at J325, J320, J321, J322, J323. Are they ~1.8V?
NO
Make sure there are no shorts on Z300. If OK, change UPP
YES
YES
Measure COL 1-5 (P1-P5) signals between UPP and keypad at J331, J324, J337, J326, J327, J328, J329. Are they ~1.8V
NO
Make sure there are no shorts on Z300. If OK, change UPP
END

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